

# test & MEASUREMENT WORLD

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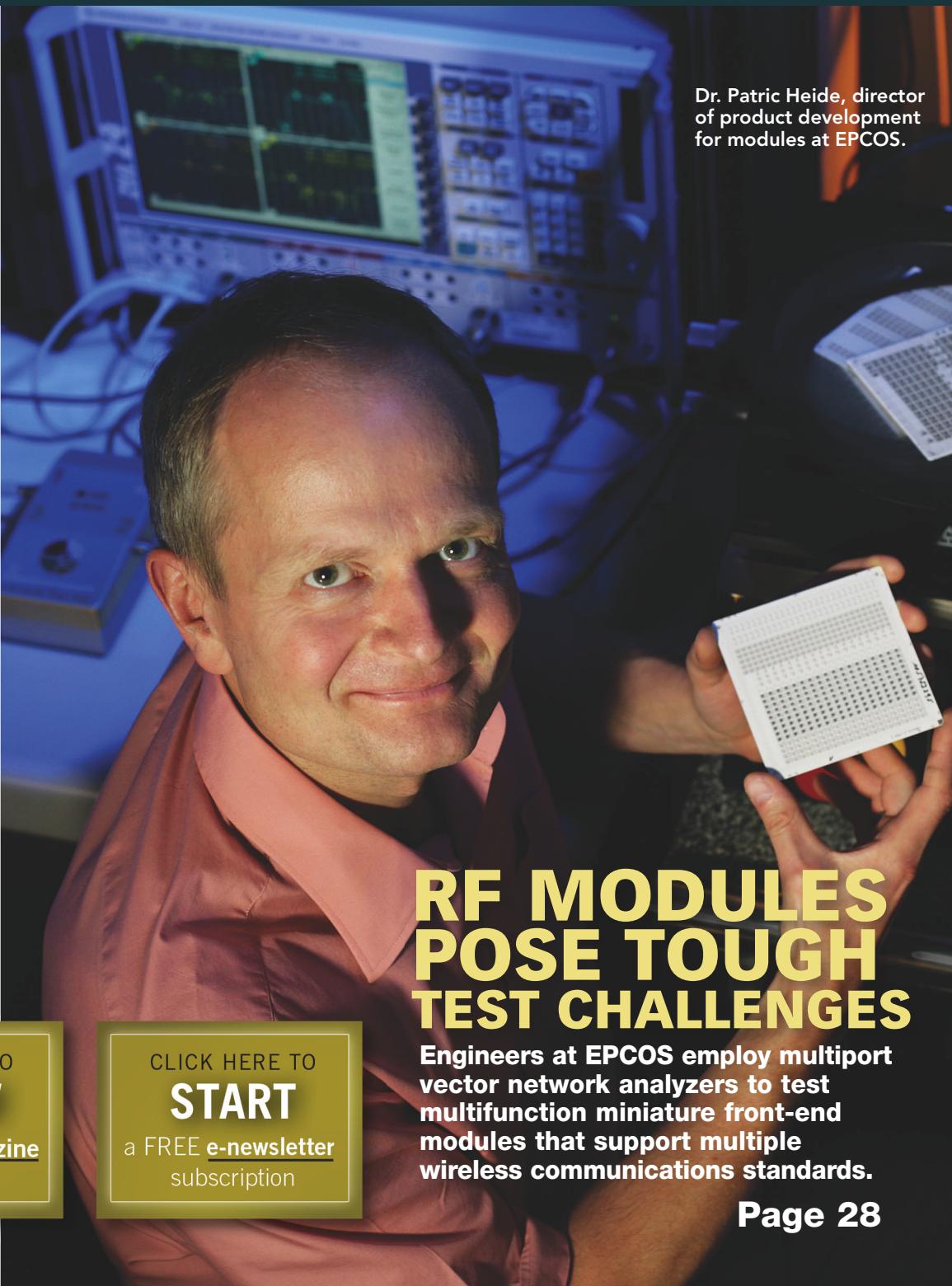
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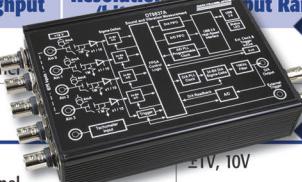
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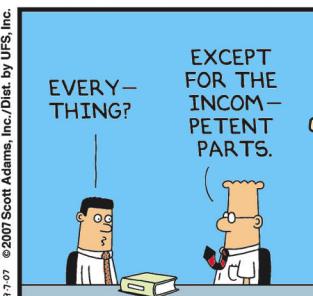
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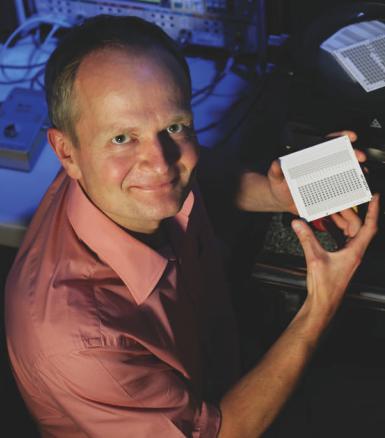


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Our editors have selected the six finalists for this annual award. To help choose the winner, cast your ballot by December 5.



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## Designing FMC-test products requires WLAN and cellular expertise

Arranging the marriage of WiFi and cellular networks is far from simple. Contributing editor Dan Strassberg writes that Agilent Technologies and Azimuth Systems have found that testing the performance of dual-mode equipment requires products designed by people familiar with both technologies.

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## Blog commentaries and links

### Taking the Measure

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### Engineering Students at Work

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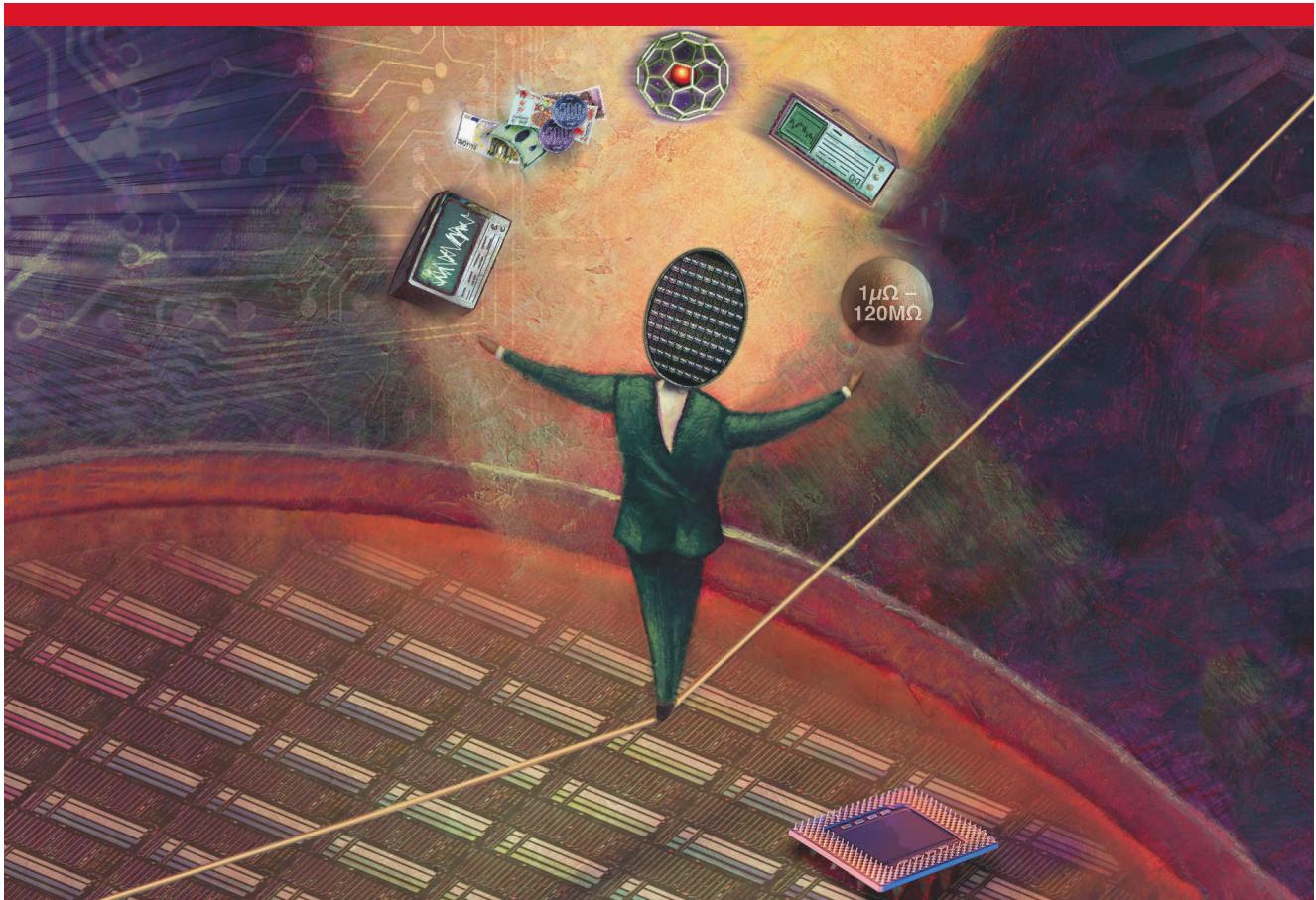
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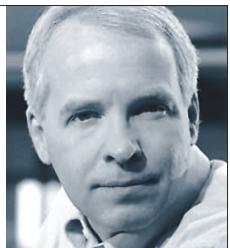


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**RICK NELSON**  
EDITOR IN CHIEF



## Innovation should be focus of next president

**T**he French philosopher and author Bernard-Henri Lévy has some advice for the next US president in light of Asia's rise in strength. In a September 14 open letter on [www.huffingtonpost.com](http://www.huffingtonpost.com), he discusses America's declining manufacturing base: "The ground that was lost in the factories of Ohio and Michigan will never be recovered." But, he adds, the next president can take three steps to deal with the country's decline: ensure that the patents behind the products manufactured in Asia continue to be

"made in the USA," ensure that people continue to think that American universities "offer the best possible education for the movers and shakers of the world," and

"ensure that American banks continue to offer the most sophisticated and secure financial services to those in possession of the world's accrued profits."

Certain American financial institutions are not faring well as I write this, so perhaps innovation and education offer the next president the most promising opportunities for accomplishment. How might each candidate respond to Lévy's advice? Their answers to questions on innovation and education posed by Science Debate 2008 ([www.sciencedebate2008.com](http://www.sciencedebate2008.com)) offer some hints.

Asked what policies he would implement to foster innovation, Barack Obama states "...the US annually imports \$53 billion more in advanced technology products than we export. China is now the world's number one high technology exporter. This competitive situation may only worsen over time because the number of US students pursuing technical careers is declining." He

wants to increase funding for basic research at a rate that would double basic research budgets over the next decade. And he would make the federal R&D tax credit permanent. In addition, he writes, he would work to guarantee students access to strong science curricula "at all grade levels so they graduate knowing how science works—using hands-on, IT-enhanced education."

Responding to Science Debate 2008's question on innovation, John McCain says he is committed to "effectively protecting American intellectual property in the United States and around the globe." He says he would streamline burdensome regulations and cut "wasteful earmarks in order to allocate funds for science and technology investments." He also says, "My policies will provide broad pools of capital, low taxes and incentives for research in America, a commitment to a skilled and educated workforce, and a dedication to opening markets around the globe." He would also support STEM education programs at government scientific agencies and believes these agencies can and should play a key role in the education of future engineers and scientists.

So how do the candidates stack up on innovation? Obama's response to Science Debate 2008 is more specific, with calls to double basic research budgets and make the R&D tax credit permanent. McCain takes a look back—"In the last decade, there has been an explosion in the ways Americans communicate with family, friends, and business partners; shop and connect with global markets; educate themselves; become more engaged politically; and consume and even create entertainment"—intimating, perhaps, that progress will continue with minimal government intervention.

Perhaps what's most encouraging is that the campaigns took the time to respond to Science Debate 2008. T&MW

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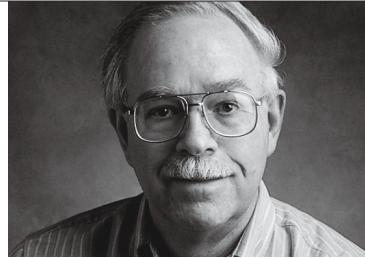
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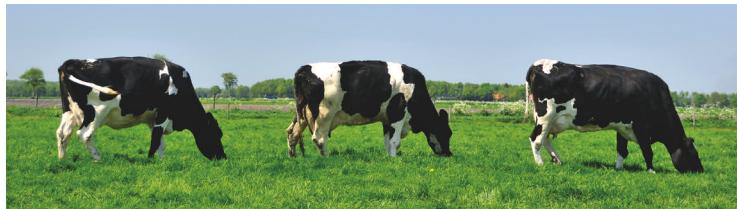


## Magnetic field sensors [sic]

We're immersed in the earth's magnetic field, but most of the time we're unaware of its presence unless we see a spectacular auroral display, or a solar-event-induced field imbalance disturbs the power grid, or we use a compass to find our way home. Magnetic fields cause problems in the test lab by affecting CRT-display alignment and color purity. Helmholtz coils provide a magnetic-field-free space for accurate evaluation of display performance.

In the June 1999 issue of *Test & Measurement World*, Jim Ericson described how to construct a magnetic-field immunity tester from PVC pipe, plywood, and a few additional components. A search for "Magnetic Field (Gauss/Tesla) Meters" on [www.tmworld.com](http://www.tmworld.com) reveals that the 2008 Buyer's Guide listed several manufacturers of measurement instruments.

Straying further afield for measuring magnetism, how about using...cows? According to an article appearing in the *Proceedings of the National Academy of Sciences* (see sidebar), domestic cattle and



certain deer species orient their bodies in a north-south direction while grazing or resting. Using satellite photos, field observations, and analysis of body impressions left by resting deer in snow fields, the authors eliminated ambient light and wind as possible influences and arrived at the earth's magnetic field as a statistically valid predictor of body orientation.

Before you purchase a herd of four-legged test instruments, though, be aware that certain maintenance requirements—power supply and by-product-disposal considerations—may present problems in an urban setting. On the other hand, availability of fresh dairy products would greatly enhance the average office's coffee break.

Anecdotes of exceptional feats of animal navigation abound. Homing pigeons seek their lofts, magnetotactic bacteria align themselves with the local magnetic field, and Monarch butterflies travel thousands of miles to their wintering grounds. Biologists pose various theories to account for these navigation feats, but devising an instrument for, say, butterfly telemetry remains a formidable challenge.

The next time you drive past a herd of cattle, check your dashboard GPS display and marvel at Mother Nature's equivalent. The chips are in the field—not the cows. **T&MW**

### MAGNETICS: AN ATTRACTIVE NUISANCE?

To read more about constructing a system to test your designs for magnetic-field effects, see: "Build a Magnetic Field Immunity Tester," by Jim Ericson, *Test & Measurement World*, June 1999: [www.tmworld.com/article/CA187497](http://www.tmworld.com/article/CA187497)

Atmospheric CO<sub>2</sub> levels momentarily spike when thousands of test engineers heave sighs of relief upon realizing that LCD displays no longer need to go through complex convergence rites such as those outlined in "TCO '99—Mandatory and recommended requirements for CRT-type Visual Display Units..." [www.d-silence.com/downloads/99crt.pdf](http://www.d-silence.com/downloads/99crt.pdf)

After reading Section 4.15 of "TV and Monitor CRT (Picture Tube) Information," which discusses the fine points of using CRT displays in the northern and southern hemispheres, you'll gaze fondly at the LCD display on your desk: [www.walshcomptech.com/repairfaq/REPAIR/F\\_crtfaq.html](http://www.walshcomptech.com/repairfaq/REPAIR/F_crtfaq.html)

Read an online abstract of "Magnetic alignment in grazing and resting cattle and deer," by Sabine Begall et al., *PNAS (Proceedings of the National Academy of Sciences of the United States of America)*, August 25, 2008: [tinyurl.com/5zpjzp](http://tinyurl.com/5zpjzp)

Training pigeons to sense changes in the geomagnetic field? Helmholtz strikes again: [jeb.biologists.org/cgi/reprint/173/1/295.pdf](http://jeb.biologists.org/cgi/reprint/173/1/295.pdf)

### TECH TIP OF THE MONTH

If you've ever had to extract numeric data from a graph that's available only in printed form, you'll want to look at Engauge, an open-source digitizer that works from a screen image and delivers data that you can drop into a spreadsheet or report. Engauge is available for a variety of operating systems, and you can download it at no cost from: [digitizer.sourceforge.net](http://digitizer.sourceforge.net)

## Johnstech contactors featured on new King Tiger testers

Johnstech International has announced that King Tiger Technology has chosen to use Johnstech Edge 400a test contactors on King Tiger's new KT-3 testers for testing DDR3, DIMM, and SODIMM memories. The companies highlighted their alliance at the Intel Developer Forum in August and at Semicon Taiwan in September.

The Edge 400a test contactors, released in July 2007, are designed to handle low-voltage (1.8-V and 1.5-V) high-speed DDR3 memory modules. The technology combines a modular design for easier component configuration and replacement and an improved warped-module-handling capability. To meet multisite requirements, standard and custom designs are available for 8, 16, 32, and 64 parallel test options. The Edge 400a contactors are also used in DIMM, DDR-DDR5, and PCI/PCI Express applications.

King Tiger's KT-3 tester offers advanced programming features and high-frequency testing for DDR2/DDR3 devices and modules; it includes the firm's behavioral test technology, which enables test engineers to use actual memory-device targets—such as PCs—as test-pattern-generation sources, thus more closely replicating real-world test conditions, according to the company. [www.johnstech.com](http://www.johnstech.com); [www.kingtigertech.com](http://www.kingtigertech.com).



## IEEE, IEC to jointly develop standards

The IEEE and the IEC (International Electrotechnical Commission) have agreed to extend their existing cooperation agreement to include a procedure for the joint, parallel development

of projects in both organizations that could lead to IEC/IEEE international standards. The agreement is an addendum to the original IEC-IEEE Dual Logo Agreement, signed in October 2002, that described a procedure for the submission of IEEE standards to the IEC for approval.

Under the new agreement, the two organizations may jointly develop standards by consulting to establish the need for new standards projects, initiating a joint development project, preparing and circulating draft standards, and voting to approve those standards. The agreement also includes processes for maintenance of approved standards to keep them up to date, as well as details on publication, copyright, and sales.

"This new procedure will allow both IEEE working groups and IEC Technical Committees to jointly develop standards in the same field while sharing information and development from all parties," said Terry deCourcelle, director of the IEEE-SA Governance & International Standards Programs. "This type of international cooperation is critical for the development of future standards that will be accepted by the worldwide technical community." [www.ieee.org](http://www.ieee.org); [www.iec.ch](http://www.iec.ch).

## LeCroy jumps into basic oscilloscopes

The WaveAce series of DSOs (digital storage oscilloscopes) from LeCroy takes aim at the Tektronix TDS1000B/2000B and the Agilent DSO3000A with six 2-channel models from 60 MHz to 300 MHz. All models feature color displays and memory depth of 4 ksamples/channel (WaveAce 100, two models) or 8 ksamples/channel (WaveAce 200/300, four models).



To help you view and analyze waveforms, the WaveAce series let you zoom in by pressing the time/div button. Once you've captured a waveform, you can use the 32 measurement functions, which include phase delay, timing, addition, subtraction, and fast Fourier transforms, and you can also perform mask

pass/fail testing. Digital filters include low pass, high pass, band pass, and band stop. A wave-sequence recorder lets you view up to 2500 screens for later replay. In addition, the WaveAce can store up to 20 waveforms and setups in nonvolatile memory.

Acquisition modes include real time, equivalent time, averaging, and peak detect. Sample rates range from 250 Msamples/s to 2 Gsamples/s. All models in the series include USB and RS-232 interfaces and PC software.

Price range: \$950 to \$2290. LeCroy, [www.lecroy.com](http://www.lecroy.com).

Editors' CHOICE

## 7 layers now performs HSUPA tests in US

Rohde & Schwarz recently announced that the 7 layers test lab in Irvine, CA, has upgraded its WCDMA test equipment from Rohde & Schwarz and will now have the ability to perform HSUPA (high-speed uplink packet access) tests. 7 layers operates indepen-

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## PCI Express frame grabber captures 16 channels

Sensoray has extended its line of OEM video-capture cards with the release of the Model 817 PCI Express JPEG frame grabber. The PCI Express x1 card captures 16 separate channels of compressed JPEG or uncompressed bit maps at 480 total fps. To provide capture flexibility, the board permits all capture parameters to be set independently for each capture channel. The Model 817 supports x1 or wider (x4, x8, x16) PCI Express slots.

An internal 16x4 analog cross-point video switch can route any combination of four input channels to external video monitors.

Each of the four video outputs can be individually turned on or off, allowing the outputs of multiple Model 817 frame grabbers to reach the same monitor. The Model 817 contains four identical VCPUs (video capture and processing units), each of which handles four input video channels. Each VCPU employs a four-channel video decoder to convert analog video into digital. A DSP (digital signal processor) captures digitized video and handles processing tasks such as frame decimation, caption overlay, JPEG compression, and status reporting. A software development kit for the Model 817 includes drivers and demo applications for both Windows and Linux operating systems.

Base price: \$705 each in OEM quantities. *Sensoray*, [www.sensoray.com](http://www.sensoray.com).



Editors' CHOICE

dent test and service centers in Germany, Asia, and the US for wireless communications.

The companies claim that with the new capabilities, 7 layers has become the first independent lab in North America that can run required HSUPA test cases. The 7 layers group has already gained experience with HSUPA testing and certification at its laboratory in Germany.

"In order to make 7 layers Inc. capable to offer these new services we will upgrade their existing Rohde & Schwarz test equipment, the R&S CRTU-W, R&S TS8950W, and R&S CRTU-RRM system," said Michael Gieselman, US Western Region sales manager for Rohde & Schwarz.

The R&S CRTU-W is a signaling protocol tester for WCDMA and dual-mode mobile phones that supports HSUPA. The R&S TS8950W performs transmitter, receiver, and performance tests according to the 3GPP test specification TS 34.121. The R&S

CRTU-RRM performs 3G/UMTS radio resource management tests. [www.rohde-schwarz.com/us](http://www.rohde-schwarz.com/us); [www.7layers.com](http://www.7layers.com).

## CALENDAR

**Vision 2008**, November 4–6, Stuttgart, Germany. Produced by Messe Stuttgart. [www.messe-stuttgart.de](http://www.messe-stuttgart.de).

**Electronica**, November 11–14, Munich, Germany. Produced by Messe München. [www.electronica.de](http://www.electronica.de).

**AeroTest America**, November 18–20, Ft. Worth, TX. Produced by Leading Edge Events. [www.aerotestamerica.com](http://www.aerotestamerica.com).

To learn about other conferences, courses, and calls for papers, visit [www.tmworld.com/events](http://www.tmworld.com/events).

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# SHOW HIGHLIGHTS

## Calibration at Disney World

>>> **NCSL International Workshop and Symposium, Orlando, FL, August 3–7, [www.ncsli.org](http://www.ncsli.org).**

The 2008 NCSL symposium began with a keynote address by Dr. Richard S. Davis with the International Bureau of Weights and Measures. Davis explained why the kilogram, the last standard of the International System of Units, is still an artifact. “It’s only a matter of time until we redefine the kilogram,” he said.

In a technical session, Dean Jarrett of NIST (National Institute of Standards and Technology) discussed measurement methods and NIST traceability paths for high-resistance measurements. He showed a measurement system that lets a primary standards lab use a teraohmmeter to transfer resistance from NIST. George Jones of NIST discussed power loading of 1- $\Omega$  resistance standards. He found that reference resistors were producing different values depending on the excitation current.

Paul Roberts of Fluke explained how phase noise affects the calibration of RF spectrum analyzers. He discussed how the different components of a spectrum analyzer contribute to overall noise as you move away from a carrier.

Dr. Li Pi Su from the US Army Primary Standards Lab reported on a comparison of vector network analyzer measurements conducted at the three primary standards laboratories of the

US Department of Defense and two industry labs. The method involved calibrating four attenuators at frequencies from 1 GHz to 26.5 GHz.

Steven Stahley of Cummins discussed the construction of a new metrology lab. He cited issues with location, lab planning, and unforeseen circumstances in his presentation.



**Keithley's 2636 SourceMeter makes low-current, high-resistance measurements.**

Courtesy of Keithley Instruments.

### ON THE EXHIBIT FLOOR

**Fluke** showed an RF calibration system for spectrum analyzers for frequencies above and below 4 GHz. The company's Hart Scientific division exhibited blackbody sources for calibrating infrared thermometers. **Keithley Instruments** exhibited the 2636 SourceMeter, for low-current, high-resistance measurements, and its latest bench multimeter, the 6½-digit Model 2100. **Yokogawa** exhibited the DL9140L 1-GHz oscilloscope.

**Agilent Technologies** demonstrated its precision network analyzer, the E4448, used as a calibrator for RF devices such as attenuators. **Ametek** displayed a dry-well calibrator with a temperature range of -90° C to 650° C that works with an eight-channel probe scanner. **T&MW**

## EMC in the Motor City

>>> **EMC Symposium, Detroit, MI, August 19–22, IEEE, [www.emc2008.org](http://www.emc2008.org).**

At the 2008 EMC Symposium, EMC (electromagnetic compliance) consultant Doug Smith demonstrated how to use two current probes with a spectrum analyzer to find resonance in a cable, and he explained how using ferrite cores around the cable reduces the amplitude of the resonant current. Professor Keith Hoover from Rose-Hulman Institute of Technology showed experiments used to teach EMC to college juniors majoring in computer engineering. Randal Vaughn of Silent Solutions used a spectrum analyzer to show how poor shielding due to “pigtails” decreases a cable's shielding effectiveness.

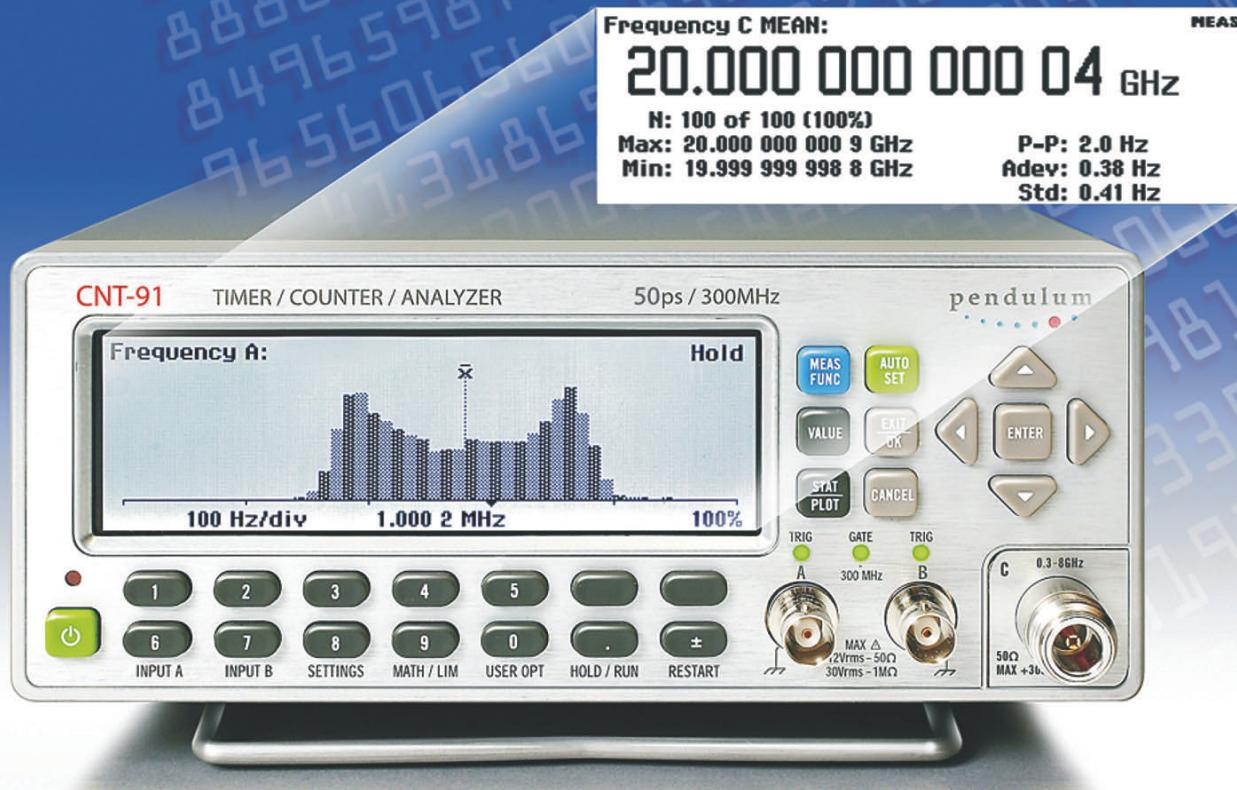
In a technical session, Professor Nathan Ida from the University of Akron covered his course for juniors majoring in computer engineering. “CE majors need an understanding of EMC as it relates to high-speed digital communications,” he said. The course covers measurements, regulatory compliance, ESD, and designing for EMC. Professor Arnold de Beer from the University of Johannesburg presented “Problematic Concepts in the Introduction of EMC.” He explained that “common-mode is a difficult concept to grasp, and it's crucial to EMC.”

### ON THE EXHIBIT FLOOR

**Agilent Technologies** unveiled an EMC option for its MXA and EXA signal analyzers, which adds CISPR emissions limits, an RMS detector, a quasi-peak detector, EMI averaging, noise-figure measurements, and phase-noise measurements. **Teseq** exhibited several new products including the AES 5500, an automotive transient emissions test system. **LeCroy** demonstrated an EMC option for its WaveRunner Xi 2-GHz oscilloscopes.

**AR Worldwide** introduced the CER 2018A EMI receiver and PL7004 laser-powered probe for characterizing chambers. **ETS-Lindgren** has added several EMI antennas to its portfolio. The Model 3142D BiConiLog covers 26 MHz to 6 GHz, and the Model 3180 mini-biconical antenna covers frequencies from 30 MHz to 1 GHz. **Amber Precision Instruments** exhibited an EMI immunity scanner system consisting of a mechanical arm that scans a radiating probe over a PCB assembly. **Rohde & Schwarz** introduced the ESL precompliance EMI test receiver. Two models range from 9 kHz to 3 GHz or 9 kHz to 6 GHz. **T&MW**

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### USB 3.0 is coming

With 64-Gbyte flash drives and terabyte external hard drives now available, USB 2.0 has become a data bottleneck. USB 3.0, with its 5-Gbps bit rate, will change that. If you plan to develop USB 3.0 products and you're not currently testing other high-speed buses such as PCIe (PCI Express) Gen2 or SATA-3 (Serial ATA III), start making a case to your manager for a faster oscilloscope.

USB 3.0 will leverage technology from PCIe Gen2 (5-Gbps) and SATA-3 (6-Gbps) serial buses. It will use 8b/10b data encoding, which reduces the data throughput rate to a maximum of 4 Gbps. "In practice," said Mike Engbretson, USB test solution marketing manager at Tektronix, "the data throughput may be around 3 Gbps." Still, the 5-Gbps bit rate is more than 10X faster than USB 2.0. (The online version of this article contains a link to a discussion with Engbretson, covering USB

3.0 technology in more detail, [www.tmworld.com/2008\\_10](http://www.tmworld.com/2008_10).)

Like PCIe Gen2, USB 3.0 will use a 2.5-GHz fundamental clock frequency. So, you'll likely need a 12.5-GHz oscilloscope if you need to see a signal's fifth harmonic. USB 3.0 will also require you to measure a signal at the receiver, which isn't necessary for USB 2.0. With the higher bit rate, USB 3.0 receivers will need equalization at the receiver because the signal eye will be closed after traveling through PCB traces, connectors, and cables.

Just how much oscilloscope bandwidth you'll need is still open to debate. Jim Choate, product management engineer at Agilent Technologies, suggests that using a 10-GHz oscilloscope at the receiver will reduce the amount of jitter and noise you'll see

because some noise is generated by the instrument itself. "There's very little high-frequency content at the receiver," he said.

Engbretson countered that you'll need 12.5 GHz to capture the signal's fifth harmonic and that using a lower-



USB flash drives such as the Kanguru FlashBlu now hold up to 64 Gbytes of data. Courtesy of Kanguru.

bandwidth oscilloscope will reduce the amplitude of the measured signal. Engbretson, Choate, and Mike Michelletti, senior product marketing manager at LeCroy, agree that you'll need to use a 12.5-GHz oscilloscope at the transmitter.

Sample rate will be equally important because of the USB 3.0 signal's rise time. "At the transmitter," noted Choate, "edges will rise in less than 70 ps." You'll need a sample rate fast enough to measure the signal's rise time.

"The USB 3.0 specification could specify a 50-ps minimum rise time, although actual hardware may not reach that speed," said Steven Sanders, product development engineer at LeCroy.

USB 3.0 should have a specification version 1.0 in time for a USB developer's conference in November. Initial USB 3.0 interface ICs and consumer products should appear in mid-2009, with widespread deployment in 2010. You can expect the first USB 3.0 products to be data-storage devices such as flash drives, external hard drives, digital music players, and digital cameras. After that will come video products and, eventually, data-acquisition systems that need the high data throughput. **T&MW**

### Programmable power supplies

Lambda's NV-350 and NV-700 series programmable power supplies provide up to 350-W and up to 700-W continuous output, respectively. Both series are 1U high and operate from 90 VAC to 264 VAC. Outputs are 3.2 V–3.6 V at 40 A and range up to 24 V–26.4 V at 25 A. [www.lambdapower.com/products/nv-series.htm](http://www.lambdapower.com/products/nv-series.htm).



### Oscilloscope consulting service

Amherst Systems Associates (ASA), maker of M1 oscilloscope software, has started a consulting service to help you choose an oscilloscope. ASA's ScopeMatch program can keep you from buying more oscilloscope than necessary. ASA will discuss signals, probing, software, and oscilloscope specifications with you. [www.amherst-systems.com/scope-match.htm](http://www.amherst-systems.com/scope-match.htm).

### Instrument software for PC sound card

FreeView-Sound-Pro from Hacker Technology turns your PC sound card into a datalogger, chart recorder, oscilloscope, or FFT analyzer. With an eight-channel sound card, the software can operate on all eight channels at the full speed and resolution of the card. It can store data files up to 2 Gbytes and operates with Windows 95 through Vista. [www.hacker-technology.com/100493.html](http://www.hacker-technology.com/100493.html).

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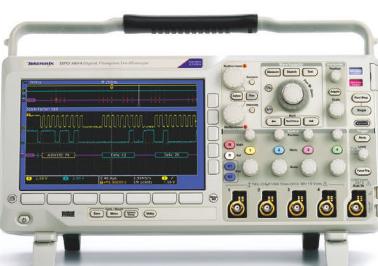
DPO70000/DSA70000 Series  
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TDS1000/TDS2000 Series  
40 to 200 MHz



DPO7000 Series  
500 MHz to 3.5 GHz



DPO3000 Series  
100 to 500 MHz



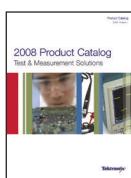
DPO4000/MSO4000 Series  
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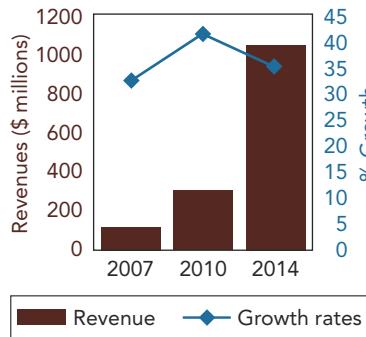
## Demand grows for multiple-services testing

There is a prevailing trend in the telecommunications industry to offer VoIP, data, and IPTV services over a single converged network. The integrated triple-play test-equipment market registered revenues of \$121.1 million in 2007—an increase of 32.1% from 2006. Revenues will likely reach more than \$1 billion in 2014 at a compound annual growth rate of 36.0% from 2007 to 2014 (figure).

Triple-play networks must support multiple technologies as well as a variety of standards and protocols. There are currently five VoIP protocols in use and three different ways to deploy IPTV and VoD (video on demand).

Successful test equipment will likely test new network elements entirely to ensure that they will work as designed. A monitoring system must be capable of capturing and decoding media and signaling information, which means it must also support a wide range of technologies, protocols, and standards.

The main challenge for a service provider is getting breadth of coverage by having all multiplex services in



Total market revenue for the global integrated triple-play test-equipment market from 2007 to 2014.

place. Test-equipment vendors have to pay careful attention to the industry in order to offer cutting-edge test and monitoring systems that fulfill the end users' needs.

Network optimization also challenges service providers. Network operators must optimize their networks to handle new services and applications that impact the bandwidth, routing, and traffic flows. With IP video services such as IPTV and VoD,

the need to understand the real-time performance of a network increases. Operators try to fully optimize their networks in order to reduce unnecessary capital expenditures and save money, but the lack of appropriate network optimization tools is a current challenge.

Consolidation remains a challenge to the growth of the integrated triple-play test-equipment market. As the telecommunications industry continues to consolidate, test-equipment vendors have fewer companies available with which to do business. Major test-equipment vendors such as Spirent Communications, Ixia, and Tektronix continue to overcome this problem by developing business relationships and consistently supplying high-quality test and monitoring equipment.

With the introduction of converged networks offering multimedia services, network operators can no longer afford to monitor the quality of their network alone, instead, they must monitor the end-to-end quality of the service and the quality of their end users' experience. T&MW

### PCB book-to-bill

For rigid PCBs (printed-circuit boards) and flexible circuits combined, industry shipments in July 2008 increased 6.9% from July 2007 and orders booked decreased 6.9% from July 2007. Year to date, combined industry shipments are up 5.8% and bookings are up 3.6%. Compared to the previous month, combined industry shipments for July 2008 are down 15.0% and bookings are down 17.6%. The combined (rigid and flex) industry book-to-bill ratio in July 2008 was 0.94. [www.ipc.org](http://www.ipc.org).

### Semiconductor equipment book-to-bill

North American-based manufacturers of semiconductor equipment posted \$905 million in orders in July 2008 (three-month average basis) and a book-to-bill ratio of 0.83. "Orders for semiconductor equipment continue [to] reflect the pronounced cut-back in capital expenditures this year and are at the lowest levels since November of 2003," said Daniel

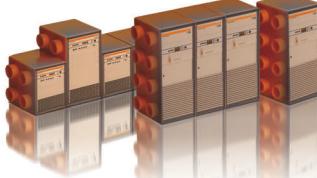
Tracy, senior director of industry research and statistics at SEMI. "While chipmakers remain attentive to cost controls, this remains a highly cyclic industry. Factory utilization levels, unit demand growth, and planned fab projects suggest that new investment activity will resume in 2009." [www.semi.org](http://www.semi.org).

### Ultra-mobile devices to outsell PCs

Ultra-mobile computing devices could far outsell desktop and notebook PCs in the long run, and mobile devices are garnering much attention from semiconductor firms, reports In-Stat (the market-research firm owned by T&MW's parent company). Intel, In-Stat reports, is gearing up to do battle with ARM—the RISC-based incumbent IP (intellectual-property) company that has dominated the embedded mobile semiconductor market for consumer electronics devices for much of this decade. The firm elaborates in the \$3995 report "Unleashing the Mobile Internet: A UMD Microprocessor Perspective." [www.in-stat.com](http://www.in-stat.com).

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The CER2018A Receiver is a complete EMI test solution with continuous coverage from 9 kHz to 18 GHz. It exceeds CISPR 16-1-1 Ed.2 Oct. 2007 and features Peak, Quasi-Peak, Average and RMS-Average detectors. Easy to use, menu-driven and self calibration with internal standard.



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## INSTRUMENTS

### All measurements are estimates

Whenever you make a measurement, the result you get is an estimate of the true value. Instrument makers publish accuracy specifications, usually expressed as a percent—but a percent of what? Through the accuracy specification, the manufacturer guarantees that a measurement is within some tolerance of the actual reading. Therefore, accuracy really indicates the measurement *uncertainty*.

Here's an example using a B&K Precision Model 2707A handheld multimeter. Assume you want to measure around 10 V. The B&K 2707A has a 2000-count display, meaning that it has a range of 0 to  $\pm 1999$ . To measure 10 V with the meter's finest resolution, set the dial to 20 VDC. The measurement range is 0 V to  $\pm 19.99$  V. Now, assume you make a measurement and get a reading of 10.00 VDC. What's the uncertainty of the measurement?

B&K specifies the meter's DC accuracy at " $\pm 0.5\%$  plus 1 digit," but is that

$\pm 0.5\%$  of reading or of full scale? Unless the manufacturer specifies a percentage of reading, you must assume the uncertainty is a percentage of full scale. So,  $0.5\%$  of 20 V is 0.1 V.

Then, you must add one digit (sometimes called a count), which is 0.01 V (10 mV) on the 20-V range. Thus, the uncertainty of your measurement is  $\pm 0.11$  V. A 10.00 reading, assuming that the meter is perfectly in calibration, means that the true value can range from 9.89 V to 10.11 V.

There's a lot more to measurement uncertainty, a topic that would take many pages to cover thoroughly. For example, it's still possible to get a mea-



A 3½-digit multimeter has a display range of 0 to  $\pm 19.99$  V on the 20-V scale. Courtesy of B&K Precision.

surement reading that is outside the uncertainty range even when the actual value is within the range. Every measurement, therefore, has an associated uncertainty and a confidence level. When you have an instrument calibrated, you can request an uncertainty specification

and a confidence level that your measurements will be within the manufacturer's specifications. Remember that instruments drift over time, which increases uncertainty and decreases confidence.

*Martin Rowe, Senior Technical Editor*

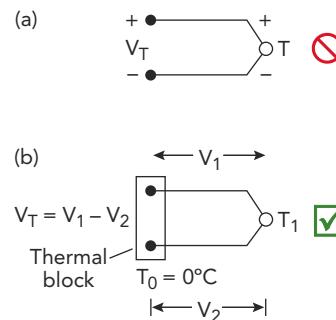
## DATA ACQUISITION

### Thermocouples often described incorrectly

Perhaps the most common mistake told about measurement is the phrase "A voltage is developed across the junction of a thermocouple that's proportional to temperature." It's repeated so often that even experienced engineers take it for granted. It's also incorrect.

A thermocouple is made two of wires of different metals where the tips are connected (often welded) to produce a good electrical connection. This junction is the temperature measurement point. **Figure a** shows the incorrect assumption about thermocouples. There is no voltage developed across the junction, although there will be a voltage across the open ends of the wires ( $V_T$ ).

In **Figure b**, assume that the thermocouple junction is at temperature  $T_1$  and, for simplicity, assume that the open ends of the wires are both at  $T_0 = 0^\circ\text{C}$ . A wire whose ends are at different tem-



**Thermocouples generate a difference voltage proportional to a temperature difference.**

peratures will produce a small voltage across those ends, called the Seebeck Effect. That voltage depends on the composition of the wire and the temperature difference across the wire's ends.

The material of a wire affects the voltage across its ends, so wires of two

different materials produce two different voltages ( $V_1$  and  $V_2$ ) for the same temperature difference. Thus, the voltage across the terminals is  $V_T = V_1 - V_2$ . *The voltage develops across the wires, not across the junction.*

Because keeping the wire ends at  $0^\circ\text{C}$  is impractical, equipment manufacturers use a circuit to measure the temperature at the ends of the thermocouple wires and electronically compensate for that temperature. It's called cold-junction compensation (CJC). Even with CJC, the thermocouple wire connections must be as close to each other's temperature as possible to minimize measurement errors. Most connections to thermocouple measuring equipment, therefore, are mounted on a thermally conductive block.

*Martin Rowe, Senior Technical Editor*

## Serial port controls ADC

Using a PC's serial port, C# code, and an ADC, you can digitize an analog signal.

By Yury Magda, Consultant, Cherkassy, Ukraine

Engineers often need simple measurement circuits that connect to a PC. When you don't have the resources to buy a digitizer for low-speed signals, you can build one yourself with just two ICs connected to a PC's serial port. The throughput rate of the digitizer depends mainly on the performance of the PC's operating system, processor speed, and memory. I was able to achieve 250 samples/s with a 2.4-GHz Pentium-based PC with 512 Mbytes RAM running Windows XP. Faster processors will produce higher sample rates. You can calculate your throughput rate by counting the number of conversions for 1 s.

The circuit in **Figure 1** shows that you can use an MCP3201 12-bit successive-approximation ADC (analog-to-digital converter) with a MAX232 RS-232 interface IC. Using an application written in C#, you can get data into a PC that runs Windows XP or Vista. You can download the source code from the online version of this article at [www.tmworld.com/2008\\_10](http://www.tmworld.com/2008_10).

The MCP3201 uses RTS (ready-to-send), CTS (clear-to-send), and DTR (data-terminal ready) serial-port lines to communicate with a PC. Its standard SPI (serial peripheral interface) port communicates to the MAX232. The analog signal connects to the MCP3201's IN+ pin, and the MAX232 converts RS-232 signal levels to TTL-compatible levels.

The digital output stream from the D<sub>OUT</sub> pin goes through the MAX232 to the serial point on the IC's CTS line. The

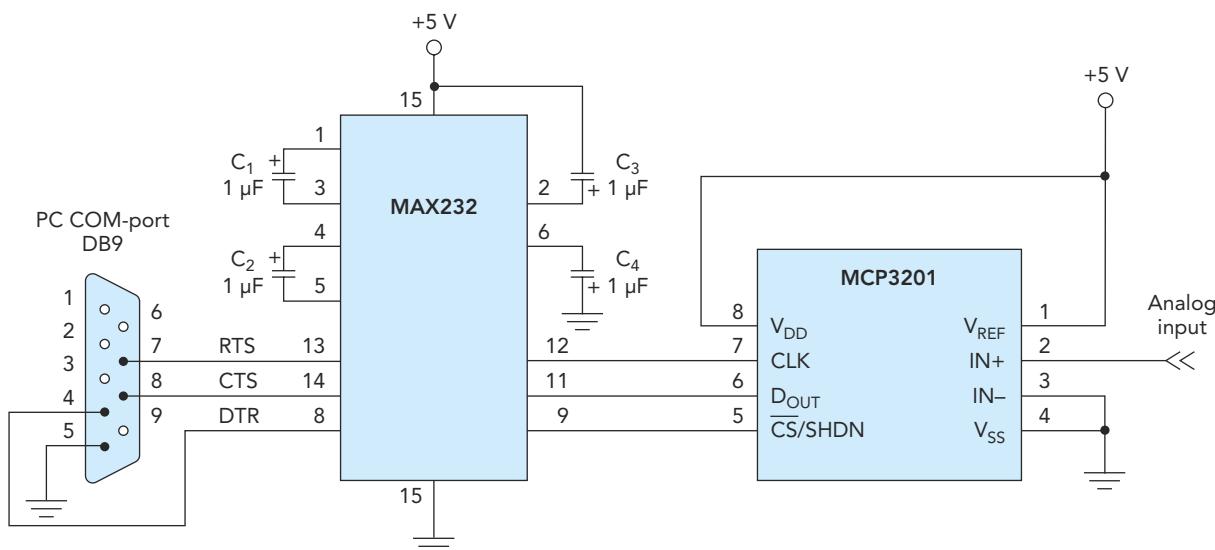
RTS line provides clock pulses to the ADC's CLK (clock) pin. Each separate bit appears at the D<sub>OUT</sub> pin on the falling edge of the CLK signal. Thus, a software application must latch the bit on the rising edge of the clock pulse. Finally, the DTR line produces the CS (chip select) signal that frames the conversion process. The CS bit must be low while the conversion is in progress. **Figure 2** shows a timing diagram of the process.

In Figure 2, the valid data bits (most-significant bit first) appear on the D<sub>OUT</sub> line after the third CLK pulse goes low. Thus, you must use software to discard the first three bits after reading the data.

The software application is written in free Microsoft Visual C# 2008 Express Edition. The built-in SerialPort component in C# provides full control over the port. The software is implemented as a simple console application. You don't need a device driver to use a serial port with this code.

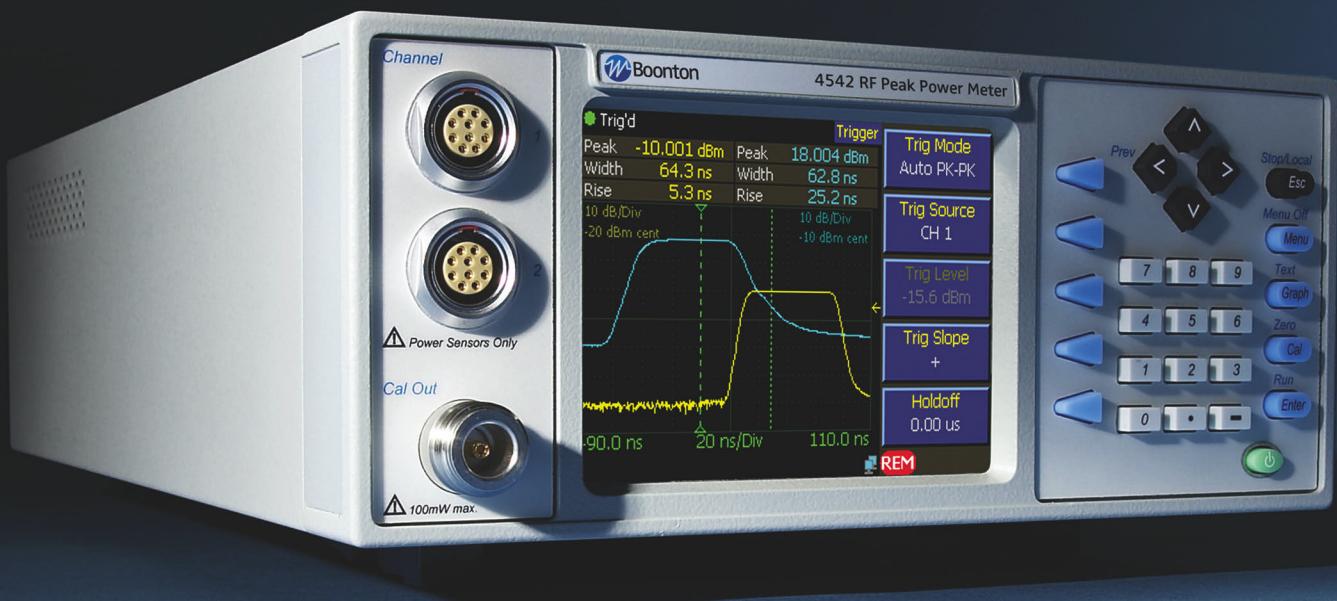
You can easily repeat or modify the source code to fit your application. For example, you can send the data from the ADC to another location over the Internet or pass data to Excel or another application for analysis.

You can also improve on the hardware design in Figure 1. For example, placing a low-pass filter in front of the ADC will reduce noise and thus reduce errors caused by aliasing. Always use a bypass capacitor on the MAX232's V<sub>CC</sub>



**Figure 1** A MAX232 IC interfaces an MCP3201 ADC to a PC's serial port.

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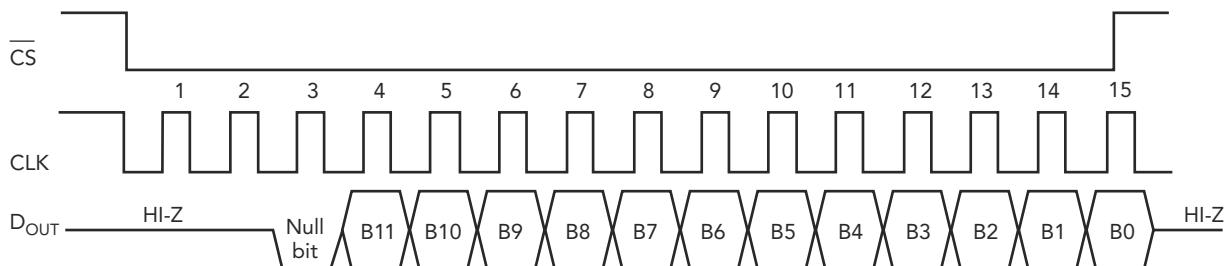


Figure 2 Software latches 15 bits, discarding the first three after reading the data.

pin. Place the 1- $\mu$ F capacitor (recommended value) as close as possible to the device pin.

You can replace the MCP3201 with a similar successive-approximation ADC that also has an SPI-compatible interface. For instance, you may use a Linear Technology LTC1286 or LTC1297. If you plan to use a different ADC,

you will need to make some hardware modifications, so check the manufacturer's data sheet for details. Instead of a MAX232 line driver, you can use similar parts such as MAX225 or MAX233.

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These parts don't require any external components, thus simplifying the design.

If you use other hardware, you may need to modify the application source code, too. As an example, you may need to change the `for (int i = 0; i < 15; i++)` loop statement in the source code according to the timing diagram of the part you select. T&MW

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# VOTE for the 2009 Test

**Our editors have selected the six finalists. To help choose the winner, cast your ballot by December 5.**

**A**t a time when global competition is tougher than ever, product quality and attractive prices win the day for manufacturers. And the technical professional at the center of delivering both benefits is the test engineer.

In development labs, test engineers devise the tests that validate the functions of new features designed to make products distinctive. In manufacturing, too, test engineers must select systems that will ensure product reliability while at the same time meeting the throughput requirements needed to keep costs in check.

To acknowledge the essential role that test engineers play at every stage of a product's life—from R&D to field test—*Test & Measurement World* is presenting its sixth annual Test Engineer of the Year award. Thanks to the sponsorship of

## MEDICAL

**Eddie Abshire**

St. Jude Medical

Ninety million people in the US suffer from chronic pain, often associated with failed back surgery. While many patients resort to medication, which can lead to dependency, an increasing number now get effective relief from implanted pacemaker-like devices that deliver neurostimulation to control the pain.

ANS, a division of St. Jude Medical, this year gained FDA approval for the Eon Mini, said to be the world's smallest neurostimulator for such applications. Slightly larger than a silver dollar, the device is more comfortable for patients and requires a smaller incision. A key figure in that development effort was Eddie Abshire.

The senior test engineer, whose 21-year career includes work in missile systems for Texas Instruments, helped verify low-level firmware and electrical circuitry of the Eon Mini early in the project and worked closely with chief engineers to characterize the functionality of the implant and uncover problem areas. He then leveraged this knowledge to develop system-level tests to ensure correct functionality between the implant, charger system, and programming software.

Managers at ANS praise Abshire's skills in testing embedded software and hardware, as well as his tenacity in identifying and solving problems. Now, ANS is putting his talents to work on a new neurostimulation therapy for those suffering from depression. Said Abshire: "There's tremendous gratification in seeing a medical product getting into the marketplace and helping people."



## AUTOMOTIVE

**Jeff Greenberg**

Ford Motor

As senior technical leader at Ford Research & Advanced Engineering, Jeff Greenberg has focused on devising ways to test perhaps the most overlooked part of the vehicle system: the human driver. Since 1989, he has led teams that have built four generations of advanced driving simulators that allow people to drive vehicles in a virtual environment. "The biggest value of simulators is having a place to study the customer before the car is ready," said Greenberg.



The latest of these simulators is VIRTTEX (VIrtual Test Track EXperiment). Enclosed in a 24-ft-diameter, carbon-fiber dome, the simulator features a full-sized vehicle cab and six-degrees-of-freedom motion. Drivers see the world via life-sized, computer-generated images and feel the motion from six 64-in. hydraulic actuators that move the entire dome based on a mathematical model of vehicle dynamics.

Greenberg has led teams that have used the simulator to develop active safety systems, including forward-collision and lane-departure warning systems. The simulator required an enormous amount of data collection and analysis, including video capture of driver response, a data-acquisition system involving several hundred channels, a network analyzer for CANbus, and a fiber-optic shared cable ring throughout the lab.

The biggest challenge? "System integration," said Greenberg. "Your success depends on how well you've married the subsystems, such as data acquisition, motion, and graphics."

## CONSUMER ELECTRONICS

**Vince McGarry**

Seagate Technology

In the sharply competitive disk drive business, Vince McGarry is described by Seagate managers as "a consummate test engineer," with extensive knowledge of a wide range of test equipment. That makes him a logical choice for high-stakes projects, such as FDE (full disc encryption) and hybrid disk drives that incorporate flash memory.



McGarry's work on FDE required the integration of new ASICs and a deep involvement in the interaction of disk drives and operating systems. Using bus and logic analyzers, he identified major problems, such as data miscompares, and developed key debug processes.

On hybrid disk drives, McGarry created the ability to capture the bus activity on a hybrid-HDD (hard disk drive), process the data, and then analyze NAND flash versus disk activity. He also developed a method for creating a test script that exactly duplicates a captured command stream. That allows engineers to repeatedly run the same sequence on a hybrid-HDD and observe the response with varying algorithms.

A native of Ireland, McGarry got valuable experience in communications systems with the US Air Force before getting his EE degree from the University of Oklahoma. Early work included systems engineering in Ireland for Tyco Healthcare. No matter what the project, McGarry said that "I've always had a passion for hands-on work, like being very stubborn in tracking down root causes of faults in developing new devices."

# Engineer of the Year

National Instruments, the winning engineer will designate an engineering school to receive a \$10,000 grant.

*Test & Measurement World* will present the 2009 Test Engineer of the Year award at our "Best in Test" event during the 2009 APEX Show, taking place March 31 to April 2 in Las Vegas, NV. The winner will also be the subject of our April cover story.

In recent weeks, we've received nominations of leading test engineers from a broad range of fields. Our editors have selected the six individuals on these pages as the finalists for the 2009 award. Please review their profiles both for on-the-job skills and for overall contributions to the field. Then, cast your vote online by visiting [www.tmwORLD.com/teoty](http://www.tmwORLD.com/teoty), where you will find links to additional information on the candidates and their companies.



## DEVICE TEST

### **Mark Pearson**

Sanmina-SCI

An electronic-manufacturing-services giant with \$10 billion in sales, Sanmina-SCI values versatile engineers who can devise cost-effective testing strategies.



Mark Pearson, senior engineering program manager in the New Technologies and Ventures Group, fits that description well. In nearly 25 years of engineering, he has tested CCD cameras, scanners, magnetic optical disk drives, multimedia devices, and photolithography equipment.

For the last six years, Pearson and his teams at Sanmina-SCI have been testing home monitoring medical devices, consumer electronics products, and fiber security devices for virtual private networks and firewalls. And always, said Pearson, the challenge is the same: "How can we devise test strategies that will drive down costs for customers?"

For security appliances for networking companies, Pearson integrated eight-up testers to optimize throughput. This year, he designed an innovative system for testing set-top boxes for home entertainment systems. In the past, Sanmina created a tester system for every new box. Working with VI Technology, a test engineering services firm, Pearson fashioned a generic platform that is scalable and easily configurable for testing different set-top boxes. Thanks to Pearson's innovative thinking, the new four-up tester has reduced test times from several minutes to mere seconds, while saving floor space and operator costs. The approach reflects his personal approach to engineering: "Try to keep it simple."

## FUEL CELLS/MATERIALS TEST

### **Jay Sayre**

Battelle Memorial Institute

The quest to build a highly efficient fuel cell is fraught with problems, prompting PhD engineer Jay Sayre to call on his hands-on knowledge of polymers, chemistry, and testing to solve them. The reward? "We at Battelle view cells as having the potential to replace the internal combustion engine and reduce our dependence on foreign oil," said Sayre.

The materials challenge is especially tough. Observed Sayre: "Cells need a membrane technology that meets a high-temperature, low-relative-humidity, and cost-efficiency requirements of commercial products."

Even before the Battelle team developed its polymer-electrolyte-membrane chemistry, now ready for portable power applications, Sayre had to design a lab for synthesizing, fabricating, characterizing, and testing fuel cells. That task entailed purchasing a long list of test equipment as well as designing fuel-cell test stations for handling a variety of chemistries, including hydrogen-air and direct methanol. Such potentially volatile materials pose safety issues, which prompted a series of compliance steps, such as installing hydrogen detectors.

Sayre's work isn't confined to fuel cells. During his eight-year Battelle career, the former Virginia Tech varsity football player was instrumental in developing composite armor for the military and a "self-healing" polyurethane guard rail that gradually regains its shape after a collision. For his many contributions, Battelle named Sayre its "Inventor of the Year" in 2006.

## SEMICONDUCTOR TEST

### **David Seiler**

National Institute of Standards and Technology

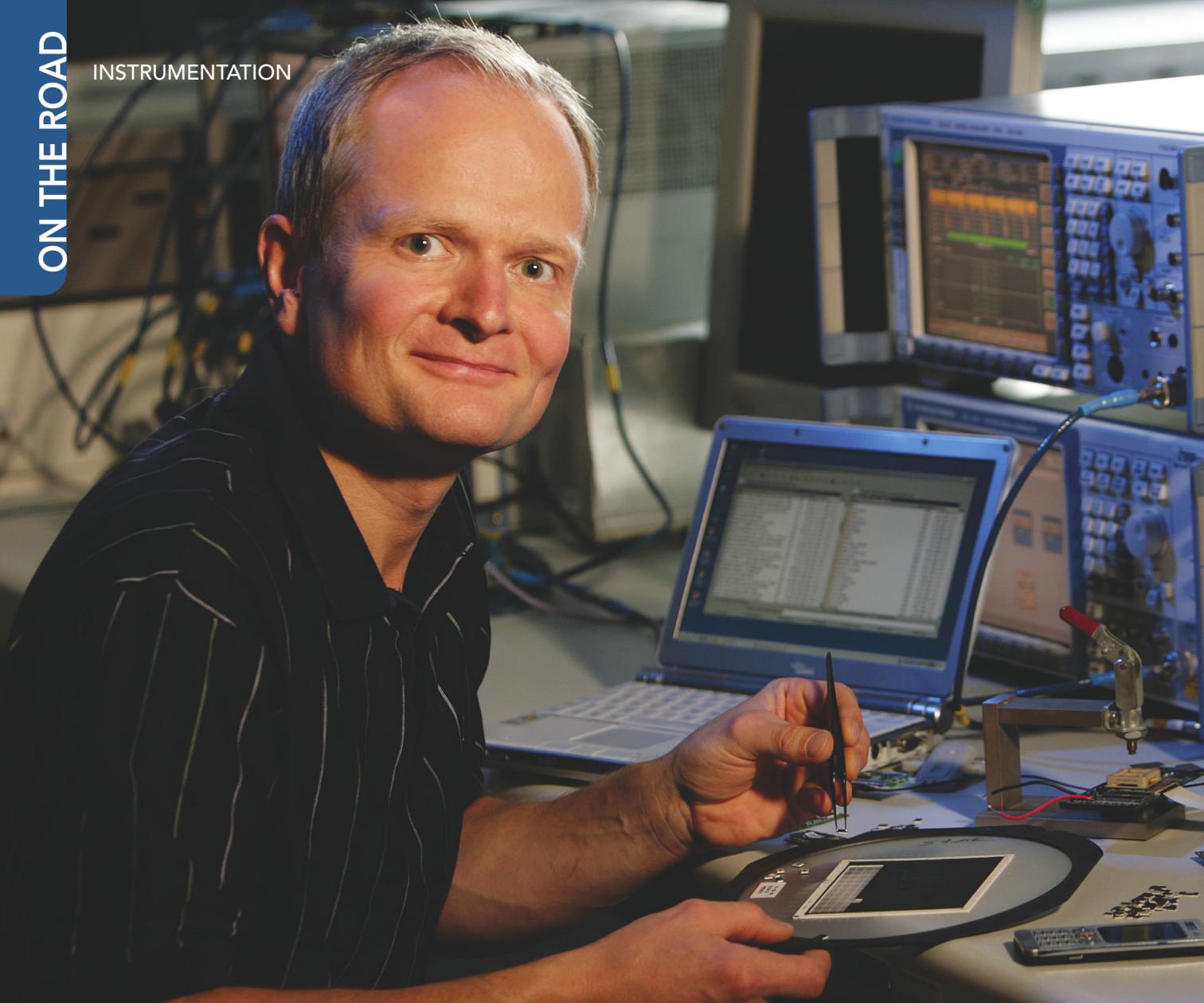
As chief of the Semiconductor Electronics Division of NIST's Electronics and Electrical Engineering Laboratory, David Seiler is responsible for tackling some



of the most pressing issues that confront the microelectronics industry. He and his team work to ensure that proper standards, measurements, and reliability test methods are in place to support current semiconductor production, and they conduct leading-edge research on future technologies.

A PhD physicist and IEEE fellow, Seiler has led many efforts at NIST, including characterizing nanoscale reference artifacts that use the spacing between atoms to measure chip dimensions. His division has also developed measurements in molecular electronics and confined silicon devices, as well as the first MEMS standards and test structures.

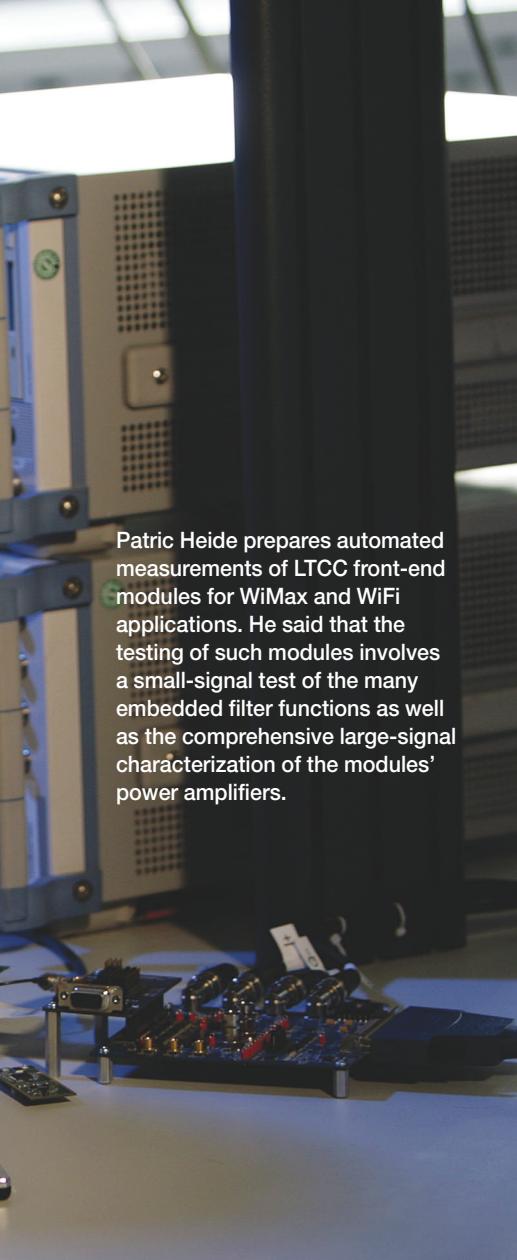
Among future technologies that his group is addressing, Seiler cites development of metrology standards for nanoscale devices, organic electronics, and "lab-on-chip" devices that marry electronics and microfluidics. Throughout such research, Seiler emphasizes the role that test plays. "We've developed one-of-a-kind testers, for instance, in power electronics for fuel cells to test silicon carbide devices at very high speeds and voltages," he said. Seiler, whose research has appeared in some 200 journals, cooperates with semiconductor firms to shape the NIST research agenda. He also works with standards organizations to ensure that NIST's measurements and test methodologies are adopted. **T&MW**



# RF MODULES POSE TOUGH TEST CHALLENGES

Engineers at EPCOS employ multiport vector network analyzers to test multifunction miniature front-end modules that support multiple wireless communications standards.

BY RICK NELSON, EDITOR-IN-CHIEF



**Patric Heide prepares automated measurements of LTCC front-end modules for WiMax and WiFi applications. He said that the testing of such modules involves a small-signal test of the many embedded filter functions as well as the comprehensive large-signal characterization of the modules' power amplifiers.**

**M**UNICH, GERMANY—The proliferation of wireless communications devices is creating a voracious demand for the RF components and modules that make those devices work. The components must, of course, be small enough to fit comfortably within the mobile wireless consumer products they populate and not crowd out ancillary functions like MP3 players and digital cameras. And because consumer products increasingly support multiple communications standards, the miniature devices themselves must incorporate the functionality necessary to implement WiFi, WiMAX, Bluetooth, GPS, DVB-H, UWB, and the various multiband cellular technologies.

On the digital side, Moore's Law has enabled vendors to make great strides in

providing increased functionality within a single CMOS integrated circuit. Radios, however, require numerous other active and passive components as well as baseband digital chips, power amplifiers, switches, and low-noise amplifiers. Discrete passive components don't follow Moore's Law and are not amenable to continual miniaturization. Christian Block, VP and CTO of the SAW division at EPCOS (see "The Evolution of EPCOS, p. 36) described the problem—and the solution—in a 2004 interview (Ref. 1). "Major progress can no longer be made by continuing to miniaturize discrete passive components alone," he said. "So we are opting for passive integration based on LTCC technology."

#### **LTCC drives miniaturization**

"LTCC" refers to low-temperature co-fired ceramic technology, which EPCOS uses to create multilayer ceramic substrates that embed passive components. Compared with the FR4 material or laminates, LTCC substrates provide lower loss and allow for the integration of many passive components in a compact space (Ref. 2).

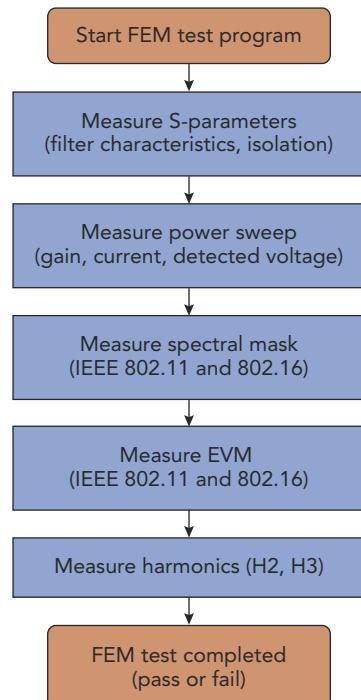
An LTCC module, said Dr. Patric Heide, director of product development for modules at EPCOS, might have anywhere from 10 to 20 layers, with each layer between 30 and 50 microns thick. Within those layers, EPCOS can build inductors and capacitors to implement filter functions and baluns. Dr. Heide explained that to help the drive toward miniaturization, the modules also accommodate semiconductor chips such as power amplifiers and switches typically fabricated in GaAs technology. "We've developed a lot of knowledge here of how to integrate these active GaAs devices with LTCC structures, and we've leveraged our experience in flip-chip and wire-bonding in order to achieve high manufacturing yields in mass production," he said.

The result of the high levels of integration, he continued, is that "we ship to our customers a fully tested RF system in a single package. In a mobile phone, you have the CMOS-based radio IC built in on one side, and on the other side you have the antenna. We provide a fully featured front-end module that goes between the two."

An example is a compact all-in-one front-end module for Bluetooth and IEEE 802.11b/g/n WLAN applications, introduced in January. The module integrates a WLAN power amplifier, a WLAN/Bluetooth switch, and a receive balun as well as bias circuitry and ESD (electrostatic discharge) protection for all RF and DC ports, yet it offers an insertion height of only 1.4 mm and occupies a footprint of only 4.5x3.2 mm<sup>2</sup> on a circuit board. Designated the D6101, it also includes a coexistence filter that allows simultaneous operation of WLAN and Bluetooth applications with all worldwide cellular standards.

#### **Multiport test challenges**

During my visit to EPCOS headquarters, Dr. Heide and his colleagues outlined the particular challenges they face in testing such modules. Dr. Jörg Schuler, who is responsible for manufacturing engineering



**FIGURE 1.** Test for a combined WLAN and WiMAX front-end module extends from S-parameter measurements through harmonic measurements. The OFDM modulation scheme of WLAN and WiMAX devices requires the measurement of EVM (error-vector magnitude) as an indication of linearity.

and testing strategies at the EPCOS SAW division, discussed the complexity of the tests needed for miniaturized, highly integrated packages with multiple RF ports: "For a GSM-quad-band WCDMA-triple-band module you have to test four GSM balanced ports, two Tx ports, three wideband CDMA ports, and one antenna. You need to test 14 ports altogether at final testing." (Each of the balanced GSM ports includes a balun that presents two ports to a test system). He said that important specifications include high dynamic range and good stop-band performance, "so your test system needs to provide as low loss as possible."

Early test systems employed by EPCOS, Dr. Schuler said, included a two-port VNA (vector network analyzer) and 12-port matrix. He added that EPCOS had early discussions with Rohde & Schwarz about test-equipment needs (see "University ties boost network-analyzer developments," p. 32). The discussions ultimately led to today's use of an eight-port R&S ZVT VNA, which supports test coverage up to 20 GHz, combined with a 10-port matrix. The combination, he said, results in fewer switches connected to the unit under test, thereby minimizing loss, increasing dynamic range, and providing

for a more accurate measurement.

Also important, according to Dr. Schuler, are fast calibration times, preferably with calibration able to be performed onsite. "What we use today is a 16-port calibration standard," he said, "which offers the possibility to automatically calibrate 16 ports in one shot—just connect test equipment to the cal standard and start the autocalibration routine. It is very practical for mass production." He added that automated calibration is particularly important at EPCOS's manufacturing plant in Wuxi, China, and he explained that with color-coded cables and connectors, an operator can quickly make the necessary connections and push a button.

### Keeping test time short

Dr. Schuler said the team needed to keep test times short despite ever-increasing levels of integration, with modules including active components that require non-

linear measurements. He added that ACPR (adjacent-channel power ratio), harmonics, and other parameters can be measured with a signal-generator and spectrum-analyzer combination, but such a test requires long measurement times over three or four power levels for a full characterization. In contrast, a VNA can quickly measure gain, the 1-dB compression point, and harmonics, said Dr. Schuler, and "The resulting test-time reduction means cost reduction for us."

CARSTEN LERP / NPN WORLDWIDE



**Jörg Schuler** says that the drive toward miniaturization and high levels of integration results in a package with multiple RF ports that presents tough test challenges.

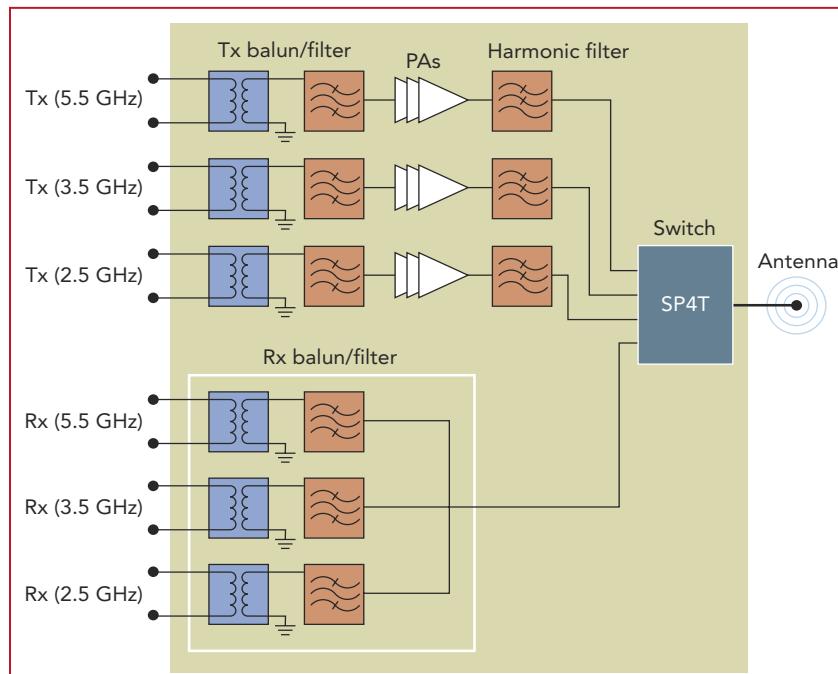
Dr. Heide described specific testing challenges

posed by highly integrated LTCC front-end modules that also include active components such as power amplifiers. He said that testing such modules involves small-signal measurement of the filter functions inside the ceramic itself as well as large-signal characterization of the amplifier functions also embedded within the module package. Specific tests vary with the application but typically include steps such as S-parameter measurement and harmonic measurements—the latter to ensure compliance with spurious emissions regulatory requirements.

**Figure 1** shows test procedure required for WLAN and WiMAX modules. A key requirement for IEEE 802.11 and 802.16 devices, Dr. Heide said, is the linearity of the transmitter operating in OFDM (orthogonal frequency-division multiplexing) format. EVM (error-vector magnitude), he added, is a key indicator of linearity. To implement a comprehensive characterization of modules under development, the EPCOS engineering lab typically employs automated PC-based test stations that include an R&S ZVA24 VNA, a customized multi-port test set, an R&S FSQ26 vector signal analyzer, and an R&S SMJ100 vector signal generator.

Dr. Heide explained that a time-consuming test procedure will not be adequate for mass production. "We cannot accept a test that takes half a minute or a minute. We need to complete the test in just a few seconds."

(continued)



**FIGURE 2.** An LTCC tri-band front-end module, implementing 2.5- and 3.5-GHz WiMAX as well as 2.5- and 5.5-GHz WiFi, includes baluns and filters; it also includes power amplifiers and an SP4T switch mounted on the RF-tested LTCC substrate.

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Testing on a sample basis to speed production is not an option. "We do a full characterization of each and every product leaving our factory," said Dr. Schuler. He added that EPCOS wanted to minimize the need for test-program adjustments when beginning production on a new module. "Our approach is always to be able to have the same test setup in the lab as we have in the test environment on the production line."

Dr. Heide said that EPCOS has recently developed a combined module (**Figure 2**) that supports all worldwide WiFi and WiMAX standards (2.5-GHz WiFi, 2.5-GHz WiMAX, 3.5-GHz WiMAX, and 5.5-GHz WiFi) in a single unit. This tri-band module operates in



Patric Heide and Jörg Schuler monitor the production-test process in EPCOS' Munich RF front-end-module manufacturing line.

four modes, he said, with WiFi and WiMAX sharing the 2.5-GHz band while the 3.5-GHz band supports WiMAX only and the 5.5-GHz band supports WiFi only.

The module consists of six baluns, three transmit filters, three receive filters, and three harmonic filters. "That's a lot

of filters to characterize," said Dr. Heide. The device also includes three power-amplifier chips and an SP4T switch. Its architecture consists of three balanced transmit and three balanced receive paths and one antenna port. As a result, there are 13 RF ports to test—a task for the R&S ZVTNA.

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### Integrating the software

Of course, multiport RF-measurement capability alone isn't enough to develop an effective test strategy. Software plays a key role, both in controlling the instrumenta-

## University ties boost network-analyzer developments

EPCOS engineers' use of Rohde & Schwarz VNAs grew out of a longstanding relationship between the two companies, according to Christian Evers, head of R&D for network analyzers at Rohde & Schwarz. He said the relationship enabled EPCOS engineers to let their Munich-based neighbor know which features they would need in next-generation test equipment. In turn, it gave Rohde & Schwarz engineers insight into which features the network-analyzer market in general might demand.

Rohde & Schwarz pioneered the network analyzer in 1950, when the company developed the first complex network analyzer—called the Zg diagram—that enabled the direct measurement of S-parameters. Evers recounted that in 1992, "We made a strategic decision to again focus squarely on the network-analyzer business—not to build a 'me too' product but a top-level instrument instead."

In pursuit of that goal, Rohde & Schwarz worked with Professor Burkhard Schiek and his students and colleagues at Ruhr University-Bochum. This relationship led to some vector-network-analysis patents, which are now owned by Rohde & Schwarz.

As it happened, Dr. Werner Faber, then head of operations of the EPCOS SAW division and now a member of the management board and CTO of EPCOS, had earned his PhD at Bochum. The affiliation that both Dr. Faber and Rohde & Schwarz had with Bochum led to a management meeting between Rohde & Schwarz and EPCOS, Evers explained. During the meeting, "We presented what we had in our basket," he continued, adding that Dr. Faber outlined what features EPCOS wanted to see in network analyzers as EPCOS embarked on its system-in-package development effort (Ref. A).

An initial success, according to Evers, came about because EPCOS test engineers needed to build matching networks to test passive components. The task was time-consuming, and the matching-network tolerances had to be accounted for in the specifications of the SAW devices under test. Evers explained that by relying on one of Professor Schiek's patents for system error correction, Rohde & Schwarz engineers were able to replace the matching networks with software developed for a network analyzer.

Other cooperative efforts followed. They included integrating Rohde & Schwarz network-analyzer software into the EPCOS production-test software platform, extending multiport capabilities to eight or more ports, and enabling multiport measurements for active components, with work continuing on true differential measurements for active components. Evers added that Rohde & Schwarz has also worked on automated calibration using a 16-port calibration standard in close association with PTB (Physikalisch-Technische Bundesanstalt, the German counterpart to NIST in the US) to ensure traceability.

Evers concluded that Rohde & Schwarz offers to work closely with all its customers, as it does with EPCOS. A close working relationship, he said, "enables us to provide exactly the new features that are needed. In turn, our customers learn how to obtain maximum output from our instruments—which is exactly what we want to achieve."—Rick Nelson

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tion and handler and acquiring and analyzing data for statistical-process-control purposes. To that end, Rohde & Schwarz engineers supported EPCOS engineers in the effort to integrate EPCOS's proprietary test software with the Rohde & Schwarz VNA software. "The big advantage for us," explained Dr. Schuler, "is that

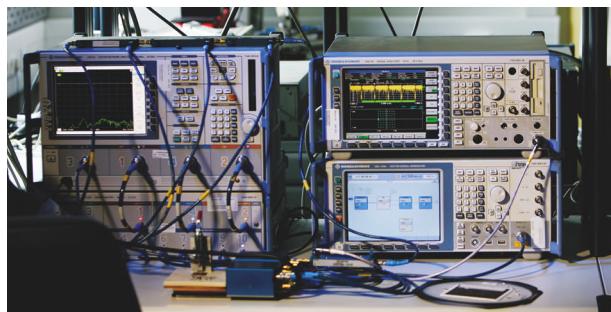


Patric Heide and Jörg Schuler discuss production-test concepts for the WiMax/WiFi front-end modules under development in the EPCOS Munich laboratory.

we have a single software interface for controlling the VNA and the switching matrix."

Despite the emphasis on Rohde & Schwarz instruments, EPCOS engineers do have in their labs instrumentation from other suppliers of measurement equipment. Dr. Heide said that this additional equipment lets EPCOS engineers ensure full compatibility and reproducibility of test results for specific measurements performed by EPCOS customers or reference-design partners, for example. These measurements sometimes use very special digital modulation schemes generated using instruments from multiple vendors.

Nevertheless, EPCOS values the established working model with Rohde & Schwarz. "It can be difficult to work with



To fully characterize the FEMs at up to 20 GHz, EPCOS engineers employ a PC-based test station that includes an R&S ZVB20 vector network analyzer, a 10-port switch matrix, an FSQ26 vector signal analyzer, and an SMJ100 vector signal generator.

a test-equipment maker without local support," said Dr. Schuler, adding that it's not easy to write down the features you expect to need in three to five years. He continued, "It's important to work interactively to take full advantage of the capabilities of the test equipment," because putting together all the pieces of the measurement puzzle requires a continuous dialog between instrument vendor and customer.

(continued)

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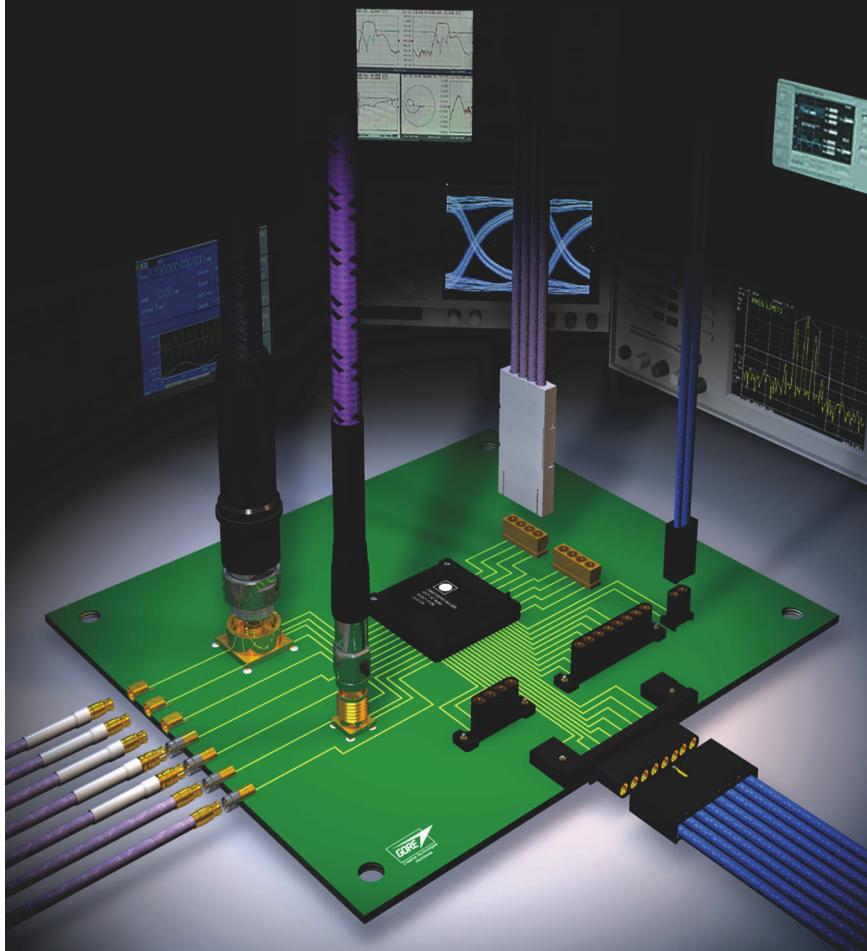
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## INSTRUMENTATION

### The evolution of EPCOS

EPCOS, formed as Siemens Components Group in 1968, evolved into the joint-venture Siemens Matsushita Components and went public as EPCOS AG in 1999. The company announced July 31 that it is pursuing a comprehensive partnership with Japan-based TDK Corp., which would result in the formation of a new company, provisionally named TDK EP Components KK. The TDK and EPCOS brands are expected to be retained.

In addition to radio front-end modules, EPCOS makes electrolytic and film capacitors, inductors, ceramic components, and SAW (surface acoustic wave) and BAW (bulk acoustic wave) filters for automotive, telecom, industrial, and consumer applications. The company has 18,300 employees and reported EUR 1.44 billion in sales for its last fiscal year.—Rick Nelson

Dr. Schuler added that through close cooperation with Rohde & Schwarz customer support, EPCOS also has the opportunity to work with products not yet on the market. "That gives us a chance to provide a lot of feedback, and it lets us make sure the instrumentation is mature when we deploy it in high-volume production." T&MW

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# PLAYING IT COOL

The semiconductor industry has long relied on scan ATPG (automatic test pattern generation) tools instead of functional test to create stimulus-response patterns with very high fault coverage. But ATPG patterns are designed to converge to high fault coverage in as few patterns as possible, making them comparatively power-hungry: Dynamic power consumption is much higher during scan testing than during normal operation. The higher-than-normal power consumption can exceed the power rating of devices and damage them during production testing or can cause false failures that require significant time and effort to diagnose. To compensate, many designers are now turning to power-aware ATPG technology to manage power during test.

## Instantaneous switching

When a logic state transition occurs in a device, numerous parasitic capacitors charge and discharge. The more state transitions that occur during a small instant of time—such as the portion of a clock cycle immediately following the rising (or falling) edge of the system clock—the higher the capacitive switching and the larger the transient currents. These instantaneous switching currents contribute to voltage drops along power rails that can add undesirable circuit delays.

Proper design of the power rails ensures that IR-drop delays arising from switching currents are within the allowable range during normal device operation. Scan ATPG patterns, however, can increase the magni-

tude of switching currents in a device by up to 10 times that of mission-mode patterns.

ATPG begins by targeting a primary fault with stimulus-pattern care bits that set up the conditions to sensitize and propagate the fault to a scan flop or primary output. The pattern generator then targets additional faults, called secondary faults, by assigning more care bits to the same stimulus pattern. Eventually, the pattern generator stops targeting secondary faults and just assigns random values to the remaining bits in the pattern to detect additional “bonus” faults not explicitly targeted by the care bits.

Both care bits and random-fill bits in each scan pattern create a large number of logic state transitions that lead to an increase in the magnitude of instantaneous switching currents in a device relative to levels that occur when the circuit operates under normal conditions. But the effects of this increase in magnitude vary depending on whether the device is in scan-shift mode or capture mode; the switching currents affect the dynamic power consumption, which is the current-voltage product measured over time.

## Shift mode

Dynamic power consumption averaged over a large number of clock cycles (such as the hundreds or thousands of cycles needed to scan a single stimulus pattern into a design while scanning out the response to the previous pattern) can lead to excessive average power, which in turn can lead to thermal problems such as hot spots on the die that can damage the device.

*(continued)*



**Power-aware ATPG technology controls thermal and power-rail-droop problems that can damage devices or lead to false failures during production test.**

BY CHRIS ALLSUP AND BILL LLOYD, SYNOPSYS

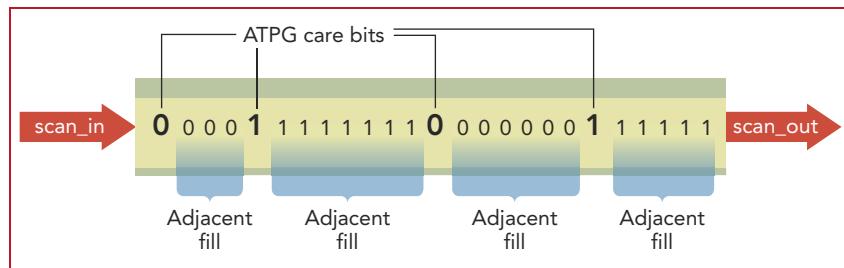


FIGURE 1. Adjacent fill replicates care bits to their nearest neighbors in the scan chain.

Power rail collapse is another shift-mode problem related to high dynamic power consumption. If transient currents are excessive during scan shifting, bits shifted into a circuit along a scan chain will be dropped, resulting in pattern mismatches on the tester. In power rail droop, which is less severe, the IR-drop delays prevent scan data from propagating to the next stage in the scan chain at the target scan-shift frequency, also resulting in test program failure.

Both excessive average power and power rail droop during scan shifting can be addressed by lowering the shift frequency sufficiently, in the latter case to allow enough time for scan signals to meet the shift cycle timing under corner conditions. The downside of reducing scan shift frequency is that it increases the time spent testing each device.

A better approach to these problems is to reduce the number of state transitions during shift. One case study of IR-drop behavior in fabricated devices showed that reducing flop switching activity during scan testing is an effective way to avoid power-related failures (Ref. 1). Methods that reduce flop switching during shift, such as the adjacent fill technique, take advantage of the fact that typically less than 10% of bits in a scan pattern are actually used to sensitize and propagate fault effects.

The adjacent fill technique, instead of random-filling the remaining bits, replicates the value of each care bit to succeeding bits in the scan chain up to the next care bit of opposite value (Figure 1). The replication of care-bit values

reduces by 85% to 98% (or more) the total flop-state transitions during scan-in sequences across an entire pattern set (Ref. 2). After capture, when data is scanned out, the flop switching activity is still significantly lower than random fill, resulting in a total combined average power reduction that is typically in the range of 50%.

### Capture mode

The most subtle and intractable power problem occurs during scan capture. Although the phenomenon is associated with both stuck-at and transition-delay ATPG patterns, it is more common in delay-sensitive at-speed testing.

During scan testing, after a pattern has been shifted in, the test clock is pulsed while the scan enable is deactivated (depending on the ATPG technique, the capture mode may include a launch sequence followed by one or more capture sequences). Excessive flop switching during the capture mode can result in enough IR-drop delay that logic values

fail to transition within the capture window, causing an otherwise “good” device to produce incorrect responses. There are few easy workarounds to resolve this problem at the tester, and tracing the source of the false-positive device failures is not a trivial task.

To illustrate the type of flop switching activity that occurs during capture mode, Figure 2 displays results from an ATPG run on a relatively small industrial design with a single clock and adjacent fill enabled during scan shifting. The graph plots both fault coverage and flop switching activity during capture (as a percentage of total flops in the design) versus pattern count, based on the power-analysis summary report produced by Synopsys’ TetraMAX ATPG product (Ref. 3).

There are two characteristics worth noting. First, although the switching peaks are higher near the beginning of the pattern set when patterns have more care bits, there is no letup in the switching “spikes” even as the fault coverage converges to its maximum. Second, adjacent fill, while effective at lowering switching activity during shift, does not limit it during capture.

In fact, high flop switching activity can occur whenever a large number of logic states change simultaneously. Regardless of whether there are few or many undetected faults remaining—or whether random or low-power fill techniques are used during shifting—the transition from scan mode to capture mode results in the most state transitions during ATPG testing.

This is because the scanned-in state is almost completely unconstrained, whereas the first clock pulse in capture mode results in a state that is highly constrained by the circuit’s state machines. Subsequent capture clock pulses, if any, almost always result in fewer state changes.

The best approach to alleviating this peak power problem is to limit the number of state transitions that occur when first entering capture mode and to use low-power fill techniques to reduce switching

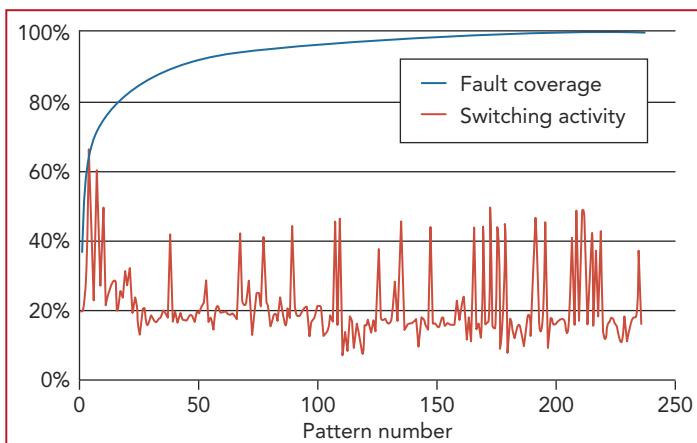


FIGURE 2. This typical profile of switching activity in capture mode illustrates two characteristics: First, although the switching peaks are higher near the beginning of the pattern set when patterns have more care bits, there is no letup in the switching “spikes” even as the fault coverage converges to its maximum. Second, adjacent fill, while effective at lowering switching activity during shift, does not limit it during capture.

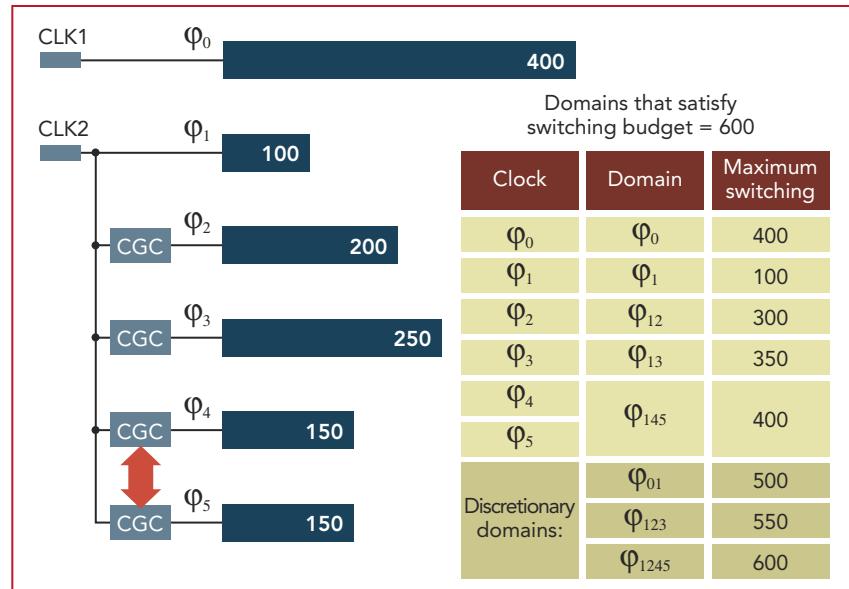
activity during shift mode. The challenge for test architects is to accomplish this with minimal impact on DFT (design-for-test) logic, ATPG run time, and pattern count.

### Clock control

To avoid an explosion in the number of test patterns and a substantial increase in ATPG run time, you do not need to minimize switching activity during capture—in fact, it's essential that you not try to do this. Instead, your goal should be only to reduce peak switching to levels that are commensurate with switching rates observed when a device operates in mission-mode. By doing this, you will suffer no unnecessary yield loss when applying the power-aware ATPG tests even under corner conditions. If the designer can determine the peak flop switching activity of a design based on simulations of mission-mode patterns, the ATPG tool can then apply constraints so the peak switching during capture mode doesn't exceed this switching budget.

Consider the example in **Figure 3** depicting a small design with multiple internally gated clocks that fan out to the indicated number of scan flops. The clocks CLK1 and CLK2 can either be external or PLL-derived. There are six internal clocks:  $\varphi_0$  and  $\varphi_1$  directly fan out to scan flops, while  $\varphi_2$  through  $\varphi_5$  are each driven by a clock-gated latch, referred to in this context as a CGC (clock gating cell). The control logic enabling the CGCs is not shown, but it is assumed that clocks  $\varphi_2$  and  $\varphi_3$  can be independently enabled and controlled by ATPG via scan-chain care bits. The two CGCs at the bottom indicate their control logic is constrained so they're mutually dependent: Whenever  $\varphi_4$  and  $\varphi_5$  are activated by ATPG, they're activated simultaneously. In addition, since CLK2 feeds all the internally gated clocks, they are each dependent on  $\varphi_1$  (though not mutually dependent).

Because of these clock dependencies, it's necessary to distinguish between the internal clocks and their corresponding clock domains, listed in the second column of the table in Figure 3. Each of these five primary clock domains can be considered independently controllable by ATPG, and each fans out to its own unique bank of scan flops with fan-out calculated in the third column. Each entry represents the maximum switching



**FIGURE 3.** This design includes six internal clocks:  $\varphi_0$  and  $\varphi_1$  directly fan out to scan flops, while  $\varphi_2$  through  $\varphi_5$  are each driven by a clock-gated latch, referred to in this context as a CGC (clock gating cell).

level for that primary domain since the number of scan flops that can change state is less than or equal to the fan-out.

While it's essential to activate all five primary clock domains to achieve maximum coverage, ATPG needs to activate only one at a time to target (and detect) any given primary fault in the design (an exception to this observation is described under “DFT requirements and exception-handling” near the end of this article). Activating more than one primary domain simultaneously to target more secondary faults with the same pattern is purely discretionary. The table in Figure 3 shows several domain combinations, referred to as discretionary domains. For example,  $\varphi_{123}$  represents the combination in which primary domains  $\varphi_{12}$  and  $\varphi_{13}$ , corresponding to internal clocks  $\varphi_1$ ,  $\varphi_2$ , and  $\varphi_3$ , are activated at the same time. Nine additional discretionary clock domains (not shown) have fan-outs ranging from 650 to 1250.

### Switching budget

Without a peak switching budget, ATPG is free to target as many secondary faults per pattern as possible by activating any combination of domains. This is the way ATPG normally behaves so it can reach the maximum fault coverage with as few patterns as possible. But with a switching budget of 600 flops, for example, the

combinations are limited: Only the three discretionary clock domains shown in the table will be activated in addition to the primary domains.

ATPG assumes there are enough independently controllable primary clock domains to meet the designer's switching budget. In general, ATPG will meet the power budget if

$$(n/F) \leq B$$

where  $B$  is the designer's switching budget expressed as a percentage of the total number of scan flops  $F$  in the design, and  $n$  is the number of scan flops in the primary clock domain that has the highest fan-out.

The fraction  $n/F$  is the theoretical maximum ATPG switching activity rate,  $C_{MAX}$ . The design in Figure 3, for example, has a maximum fan-out of  $n = 400$  flops (primary domains  $\varphi_0$  and  $\varphi_{145}$ ). The theoretical maximum  $C_{MAX} = n/F = 400/1250 = 32\%$ , so if  $B \geq 32\%$ , the power budget will certainly be met.

**Figure 4** displays two profiles of flop switching activity during capture mode for an industrial design with many internally gated clocks. The red data is associated with standard transition delay patterns, whereas the blue data reflects TetraMAX power-aware transition delay patterns. The design comprises approximately  $F = 262,700$  scan flops, and the

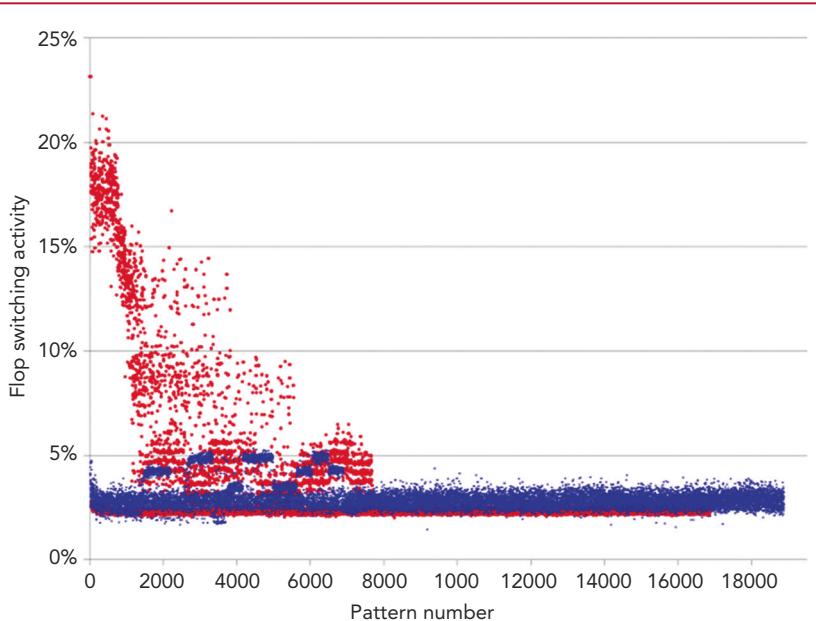
clock domain with the highest fan-out has  $n = 14,545$  scan flops. If the design's mission-mode patterns reach a peak switching level of 6%, then standard ATPG generates 1145 patterns that switch higher than this level. So, the device is at risk for incurring additional IR-drop delays that could cause scan test pattern mismatches on the tester.

In contrast, with a designer-specified flop switching budget of  $B = 6\%$ , power-aware ATPG generates patterns that all switch below this level, thereby avoiding unnecessary yield loss. You would expect to meet the switching budget since, from equation (1)

$$C_{MAX} = 14,545 / 262,700 = 5.5\% < 6\%$$

### Actual peak switching

It turns out that the actual ATPG peak switching rate  $C_{PEAK}$  for the industrial design was 5.3% with no loss in test coverage.  $C_{PEAK}$  can be less than the theoretical maximum because only a fraction



**FIGURE 4.** In these profiles of flop switching activity during the capture mode for an industrial design with many internally gated clocks, the red data is associated with standard transition delay patterns, whereas the blue data reflects power-aware transition delay patterns.

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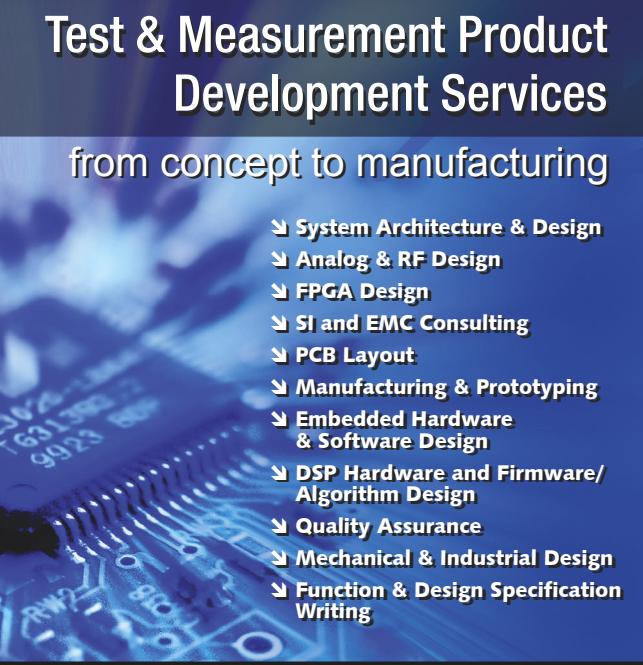

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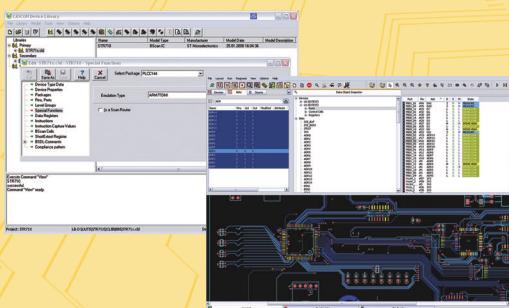
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$\alpha$  of the maximum flop fan-out  $n$  may ultimately change state. This means that ATPG could still meet a budget even if it's less than  $n/F$ . The fraction  $\alpha$  depends on the design and the type of fault model used, and it tends to be lower for transition delay tests than for stuck-at tests.

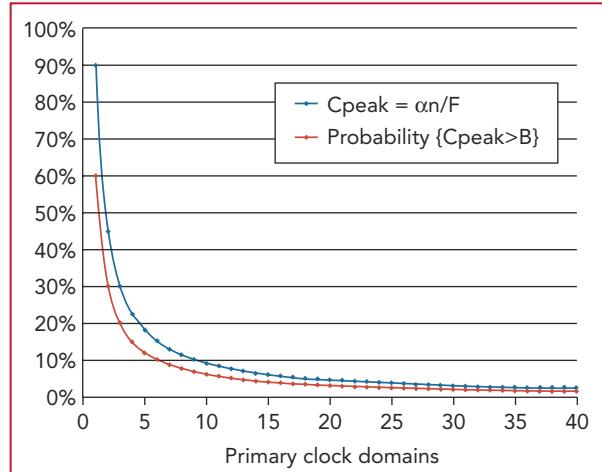
Assuming a switching budget reflects the actual peak switching level of mission-mode patterns, is it possible that ATPG's peak switching rate  $C_{PEAK}$  could exceed this budget? The answer depends on the number of independently controllable primary clock domains in the design. In the example illustrated in **Figure 5**, assume that  $\alpha = 90\%$  and the probability that  $C_{PEAK} > B$  is 60% in a single-domain scenario (as presented in Figure 2). As the number of domains increases, peak switching  $C_{PEAK} = \alpha n/F$  decreases, as does the probability that it could exceed the switching budget.

In other words, it is highly unlikely that a device having a relatively large number of primary clock domains will have peak switching levels that exceed the peak level that can be achieved by ATPG in full control of activating all these domains. Furthermore, under these conditions, there are enough discretionary domains such that  $C_{PEAK}$  approaches the theoretical switching maximum  $n/F$ . That is,  $C_{PEAK} - C_{MAX} \rightarrow 0$ .

### DFT requirements and exception-handling

The advantage of a power-aware ATPG methodology based on control of internally gated clocks is that no special DFT logic needs to be added to a design and no special DFT flows are required. Unlike ad hoc methods that require partitioning a design into separate blocks with different scan enables, control of peak power consumption is fully automated within ATPG.

Still, there are certain classes of faults that can't be detected exclusively by clock gating, and these require special



**FIGURE 5.** The likelihood that ATPG will exceed the switching budget diminishes with an increase in the number of clock domains.

treatment by ATPG to comply with switching requirements. For example, some faults can only be detected by asserting an asynchronous global reset. For these, ATPG must assign the reset value to enough flops to ensure that when the reset is asserted in the pattern, switching doesn't exceed the budget. Power-aware ATPG technology is rapidly evolving to accommodate a range of "exceptions" like this that are, in fact, routinely encountered in the design of today's complex systems-on-a-chip. **T&MW**

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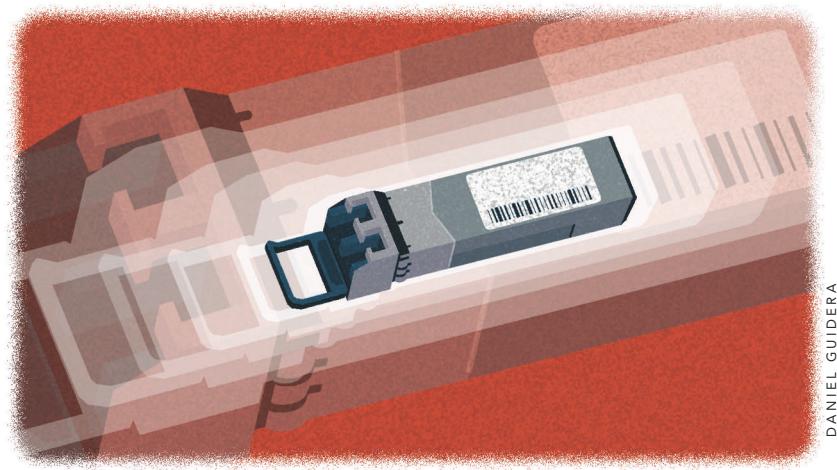
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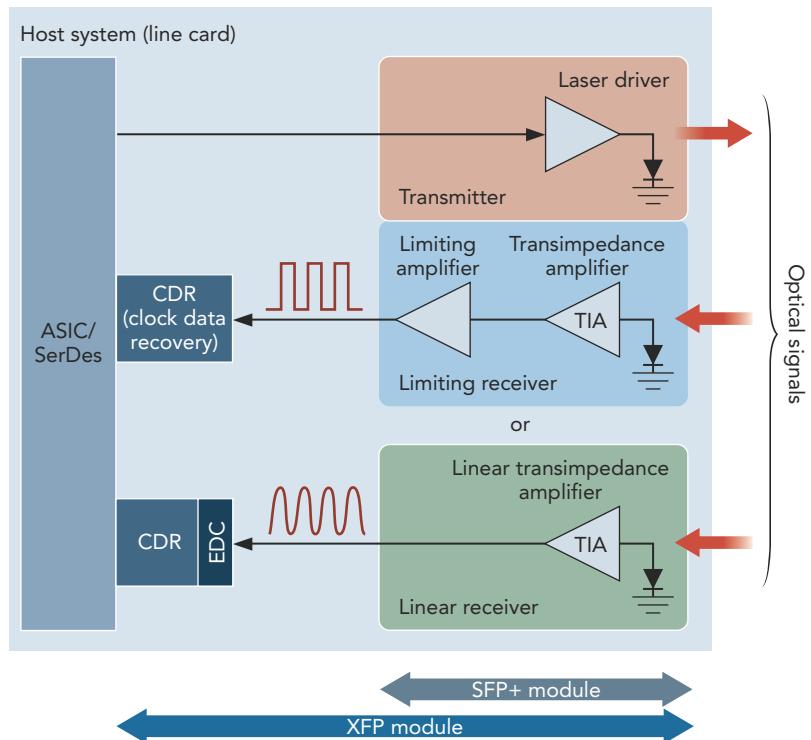
# COOPERATION to COMPLIANCE

Manufacturers of transceivers, line cards, and components find that working together helps them create Small Form-Factor Pluggable products that comply with standards.

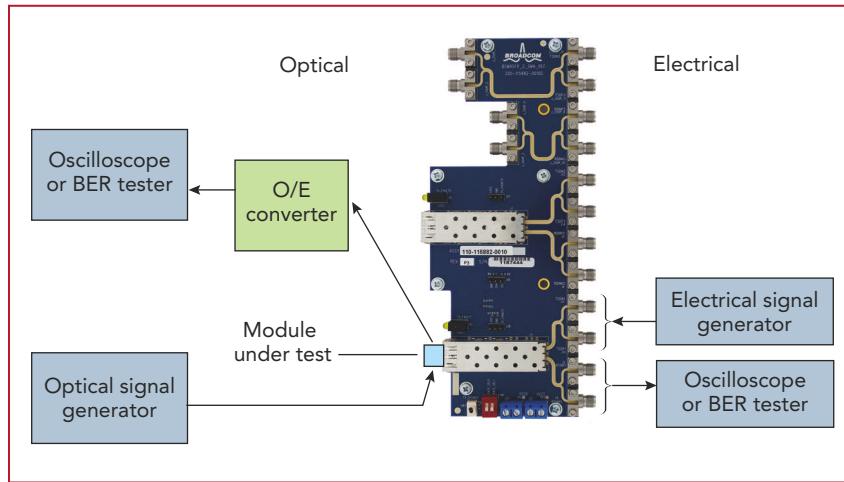
BY MARTIN ROWE, SENIOR TECHNICAL EDITOR

Large data centers such as those at Facebook or YouTube have thousands of servers that must connect through switches and fiber-optic lines. These data centers need an ever-increasing supply of 10-Gbps links to keep up with traffic. To reduce costs and save space, network equipment manufacturers need to put more links onto line cards. Because of their size, SFP+ (Small Form-Factor Pluggable) optical transceivers let line cards hold more data lines than other transceiver modules.

SFP+ modules are smaller than other transceiver modules because CDR (clock data recovery) and SerDes functions have been moved off the module and onto the line card, or host (**Figure 1**). SFP+ modules are also unusual in that they have two variants, called limiting and linear. The limiting variant includes a limiting amplifier that resets the amplitude of the signal eye. Linear SFP+ modules don't need the limiting amplifier. They send an analog representation of the incoming optical signal to the host where an EDC (electronic dispersion compensator) compensates for dispersion in the optical transmission and



**FIGURE 1.** SFP+ modules move more signal processing to the host board than other transceiver modules.



**FIGURE 2.** A module compliance board provides optical and electrical test equipment with access to an SFP+ module's ports. Photo courtesy of ClariPhy Communications.

for losses in the electrical signal. “Why two variants?” (p. 49) explains the applications for limiting and linear modules.

Both variants challenge engineers because they permit signals in the module to travel farther before they are restored to a clean form than do other optical transceiver modules. The longer path can add jitter and loss to the signal.

Testing SFP+ modules requires electrical and optical measurements. Because of the longer electrical signal channel, you must make measurements on the channel within the module and at the module's input (for transmit) and output (for receive) ports. You must characterize the channel on the host, too. Optical measurements such as receiver sensitivity and transmit jitter and power are based on compliance to standards such as IEEE 802.3ae and 802.3aq (Refs. 1, 2). Optical measurements, therefore, are the same as those for other 10-Gbps modules.

The electrical measurements, however, differ from those for other modules, and they also differ for the limiting and linear SFP+ variants. The SFP+ specification defines test processes designed to ensure a product's compliance to the specification (Ref. 3). Although some tests remain under development as of the May 8, 2008, draft, manufacturers are moving ahead with designs and production.

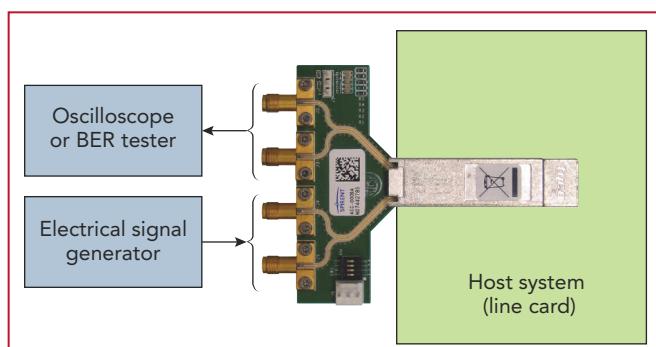
### Jitter tests need definition

The test for jitter at the output of the receive-side limiting module and at the input for the limiting host is one test that needs defining before the SFP+ standard is finalized. George Noh, senior systems engineer and senior member of the technical staff at Vitesse, explained that the current SFP+ specification for the limiting receiver calls for a maximum total jitter of 0.7 UI (unit interval) and a maximum deterministic jitter of 0.42 UI.

J-BERT, while others prefer to use an Agilent DCA-J sampling oscilloscope. The dual-Dirac method uses low-probability jitter to fit Gaussian curves to two Dirac functions from which it measures total jitter, deterministic jitter, and random jitter at a particular BER. In contrast, the DCA-J tries to find deterministic jitter by subtracting extrapolated random jitter measured in the frequency domain from extrapolated total jitter at a particular BER. Our goal in the SFP+ committee is to specify the jitter methodology that better quantifies the host receivers' weaknesses in a real system.”

Testing SFP+ modules and hosts requires the use of compliance test boards that provide test equipment with access to the module or host system under test. Compliance test boards provide standard points that provide access to modules and line cards regardless of manufacturer. **Figure 2** shows where test equipment connects to a module compliance test board. The test board's electrical signal path has known characteristics. Another option is to connect a vector signal analyzer to the module's or host's electrical transmit and receive ports and measure its S-parameters. Engineers at module makers may share their S-parameter measurements with manufacturers of line cards. Module manufacturers may also share design simulations with designers of line cards and PCBs (printed-circuit boards). Manufacturers of CDR, EDC, and TIA (transimpedance amplifier) devices also may share S-parameter data and design simulations with customers.

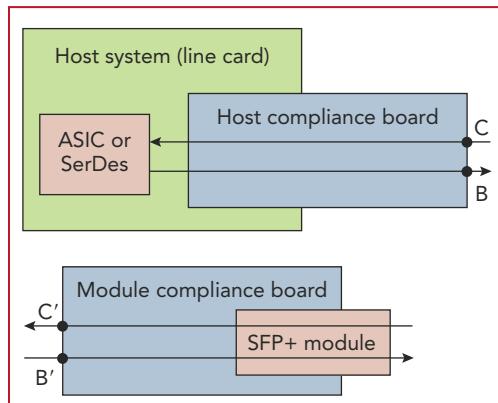
“Because of this shared responsibility,” said Rob Hannah, applications manager at Avago Technologies, “we must deliver simulations of our products to our customers.” Similarly, Vitesse, which manufactures limiting amplifiers, laser drivers, and transimpedance amplifiers, provides device data to module makers. “We swap hardware with module makers and test devices in both labs, and we analyze all signals,” said Noh. Noh will also work with line-card manufacturers



**FIGURE 3.** A host compliance board attaches to a host board, providing access for test equipment. Photo courtesy of ClariPhy Communications.

How you arrive at those numbers depends on whether you use an oscilloscope or a BER (bit-error rate) tester.

“One of the remaining open items in the SFP+ standard is how we want to measure jitter, and what limits make sense with that particular methodology,” noted Noh. “Some people prefer the dual-Dirac method using a BertScope from Synthesys Research or an Agilent



**FIGURE 4.** SFF-8341 defines test points (B, C, C') and measurements (Table 1) for the electrical paths of modules and host boards.

because Vitesse manufactures CDRs and EDCs for line cards.

In order for this data sharing to be effective, all of the manufacturers must use identical test setups for test consistency. **Figure 3** shows a host compliance test board with associated test equipment. (The SFP+ specification

shows the host and module test setups in more detail.) Designers of host boards can characterize parameters such as transmit jitter and receiver sensitivity. A vector network analyzer can also measure S-parameters looking into a host. Line-card designers can use these measurements along with those provided by module makers to verify impedance matches before designing a host.

SFF-8431 defines several tests for transmitters and receivers, including two sets of receiver measurements that cover the limited and linear variants. The document also defines tests for hosts boards. **Figure 4** and **Table 1** highlight the measurements and test points. In addition, the standard defines a calibration procedure you should follow prior to making measurements. “Calibrate before testing” (p. 52) highlights the need to calibrate a test setup.

(continued)

## Why two variants?

SFP+ has two module variants, limiting and linear. The limiting modules work with 805-nm SR (short reach) and 1330-nm LR (long reach) single-mode fiber. IEEE 802.3ae defines the Ethernet signals for SR and LR fibers, called 10GBase-SR and 10GBase-LR. The linear variant is primarily designed for legacy networks that use LRM (long-reach multimode) optical fiber, or 10GBase-LRM, based on IEEE 802.3aq. “LRM is for installations that use the older multimode fiber where network operators still want 10-Gbps speeds,” said Hannah.

LRM fiber produces more dispersion than the newer OM2/3 multimode fiber and single-mode fiber and thus requires an EDC (electronic dispersion compensator). The EDC makes the decision if an incoming bit is a 0 or 1. Because the EDC chip won’t fit in the SFP+ module, it resides on the host board. The EDC must compensate for distortions caused by everything from the remote end of the fiber, through the SFP+ module, its connector, and the copper traces on the host board. With linear modules, an analog signal from a receiver must travel along several inches of copper to reach the EDC. Distortion caused by crosstalk and impedance mismatches make the EDC’s job even harder.

Although the linear variant is mostly for LRM fibers, it can be used with SR or LM applications. “LRM fibers must use the linear variant,” said Lindsay. “But SR and LR fibers can use either. It’s possible that some line-card manufacturers will opt for linear modules over limiting modules to cut costs.” —Martin Rowe

**Table 1. Primary host and module electrical transmitter and receiver tests.**

Test	Test point (see Fig. 4)	Measurements
Host transmitter	B	<ul style="list-style-type: none"> <li>Differential S-parameters (SDD22)</li> <li>Common-mode reflection</li> <li>Termination mismatch</li> <li>Rise time/fall time</li> <li>TJ, DDJ, DDPWS, and UJ</li> <li>Eye mask</li> </ul>
Host receiver (limiting variant)	C	<ul style="list-style-type: none"> <li>Differential S-parameters (SDD11)</li> <li>Common-mode reflection</li> <li>SRS (DJ, DDPWS, and TJ)</li> <li>Eye mask tolerance</li> </ul>
Host receiver (linear variant)	C	<ul style="list-style-type: none"> <li>Differential S-parameters (SDD11)</li> <li>Common-mode reflection</li> <li>SRS (RN and WDP)</li> </ul>
SFP+ module receiver (limiting variant)	C'	<ul style="list-style-type: none"> <li>Differential S-parameters (SDD22)</li> <li>Common-mode reflection</li> <li>Termination mismatch</li> <li>Rise time/fall time</li> <li>TJ and DJ tolerance</li> </ul>
SFP+ module receiver (linear variant)	C'	<ul style="list-style-type: none"> <li>Differential S-parameters (SDD22)</li> <li>Common-mode reflection</li> <li>Term mismatch</li> <li>RN</li> <li>WDP</li> </ul>
SFP+ module transmitter	B'	<ul style="list-style-type: none"> <li>Differential S-parameters (SDD11)</li> <li>Common-mode reflection</li> <li>TJ, DDJ, DDPWS, and UJ tolerance</li> <li>Eye mask tolerance</li> </ul>

Abbreviations: DDJ—data dependent jitter; DDPWS—data dependent pulse width shrinkage; DJ—deterministic jitter; RN—relative noise; SRS—stressed receiver sensitivity; TJ—total jitter; UJ—uncorrelated jitter; WDP—waveform distortion penalty

### Transmitter tests

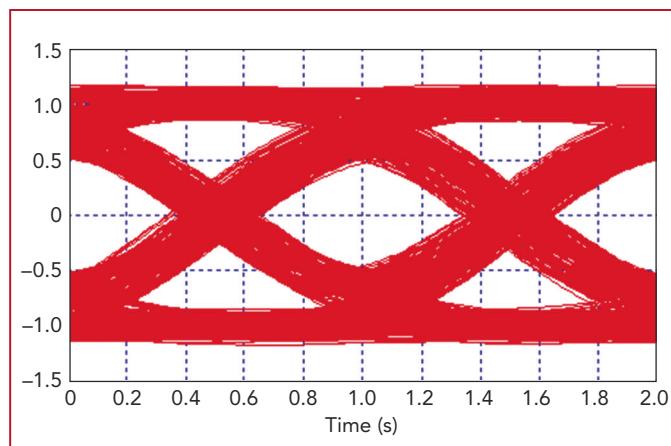
Optical tests on SFP+ transmitters are the same for both linear and limiting modules because both variants use the same transmitter circuit. Transmitter tests usually use an electrical signal such as a 9-bit or 31-bit pseudorandom bit sequence (PRBS9 or PRBS31) injected into the module through a module-compliance test board.

To perform optical measurements on transmitters, you need an oscilloscope with an optical input. Oscilloscopes that lack optical inputs require an optical receiver to convert the optical signal to electrical. Optical measurements include mask margin, extinction ratio, jitter (total, deterministic, and random), optical rise time and fall time, and RIN (relative-intensity noise).

Hannah noted that specialized oscilloscopes, commonly called digital signal analyzers or communications signal analyzers, measure these quantities through features not commonly available on general-purpose oscilloscopes. The online version of this article contains photos of equipment that engineers use for these measurements ([www.tmworld.com/2008\\_10](http://www.tmworld.com/2008_10)).

Tests that don't require oscilloscopes include TDP (transmitter dispersion penalty) for IEEE 802.3ae SR (short reach) and LR (long reach) applications and TWDP (transmitter waveform dispersion penalty) for IEEE 802.3aq LRM (long-reach multimode) applications (Ref. 4). TDP and TWDP quantify the degradation of signals caused by transmitters and fibers. TDP is a hardware setup that uses a reference receiver and BER tester to measure a trans-

mitter's effect on receiver sensitivity. TWDP tests use software to process a digitized transmitter signal. The software calculates TWDP based on calculated SNR (signal-to-noise ratio) from a simulated receiver and reference fiber.

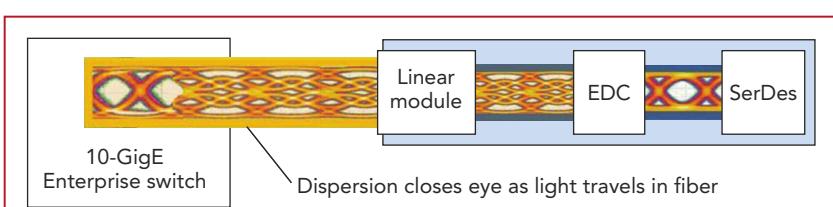


**FIGURE 5.** Limiting SFP+ modules require receiver testing with an open eye input.

To test whether the electrical signals transmitted by line cards comply with SFF-8431, you can use a host compliance board that inserts into the SFP+ cage on a line card. The compliance board's SMA connectors provide access for an oscilloscope or a BER tester. Because the CDR circuit resides on the host, the transmitted electrical signals from the line card will travel along several inches of PCB trace before reaching the host compliance board. At 10 Gbps, the digital signals from the CDR will experience distortion. Thus, to perform compliance tests on the electrical signals sent by hosts, you must measure for amplitude, jitter, and BER.

### Receiver tests

Test methods for SFP+ receivers depend on the Ethernet standard to which a module and host board must comply.



**FIGURE 6.** Model dispersion in optical fibers creates intersymbol interference that closes eye diagrams. Courtesy of Circadian Systems.

Limiting SFP+ modules need tests with an open eye per IEEE 802.3ae (Figure 5). Jitter, noise, and low amplitude add stress to the eye, but the eye opening will still be clearly visible. You must also add at least 0.3 UI of jitter in the signal. Under

these and other conditions, a module under test must pass a  $10^{-12}$  BER test.

Linear modules, which produce analog outputs, may be less familiar to digital engineers than limiting modules. Figure 6 shows how dispersion in the LRM fiber causes adjacent light pulses to interfere with each other, resulting in ISI (intersymbol interference) and a closed eye at the receiver. SFF-8431 requires that you test linear SFP+ modules for compliance using three ISI test conditions—precursor, postcursor, and sym-

metric. These three conditions simulate wave shapes (Figure 7) that often appear as a result of dispersion in LRM fibers.

Because of the closed eye, SFP+ modules can't use a limiting amplifier and need an EDC. "Ultimately, you'll see the EDC integrated into the host ASIC where its cost gets absorbed," said Tom Lindsay, principal systems engineer at ClariPhy Communications and chair of the SFF-8431 committee. "Because an open eye isn't needed, the linear TIA can potentially have lower bandwidth and thus a lower cost. Power and heat management are easier to implement on a host than on a module."

To test a linear SFP+ module, use a module compliance test board. You must observe the distortion that a module adds to the outgoing electrical analog signal. Joey Thompson, executive VP at Circadian Systems, noted that

the amount of added distortion isn't currently defined. Thus, it's important to make sure that the line card's EDC will be able to convert the incoming signal into digital form.

Testing the EDC circuit on a line card requires an electrical stressed-eye signal injected into the circuit. EDC evaluation boards, available from EDC manufacturers, let you test the device under stressed-eye conditions prior to incorporating

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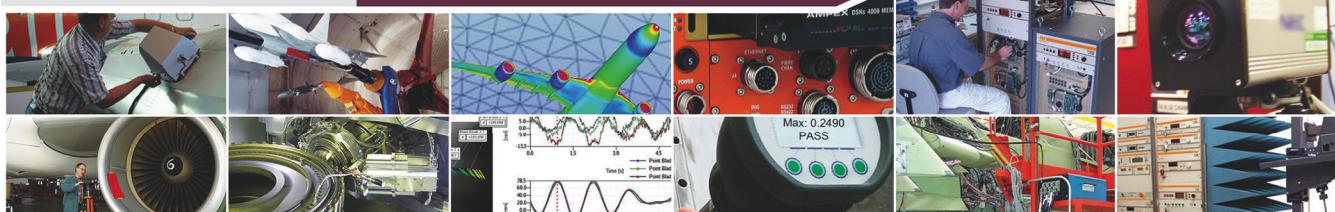
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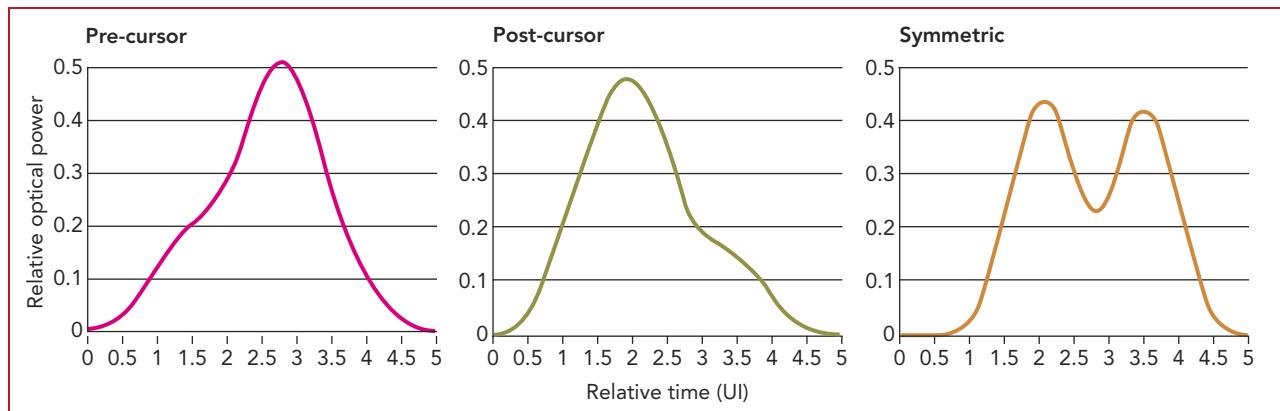
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**FIGURE 7.** Compliance tests for SFP+ modules on 10GBase-LRM fiber require three types of intersymbol interference.

them into a line-card design. SFP+ manufacturers need to test their modules with numerous EDCs and thus will use evaluation boards. Test equipment lets you create electrical or optical stressed-eye signals, letting you test the module, the EDC chip, or both as a system. To test an EDC once it's on a line card, use a host compliance board to inject stressed-eye signals.

Although some of the SFP+ specifications and test requirements are still open to debate, manufacturers are pushing ahead with creating SFP+ products

because of the economic benefits. The quest to lower costs for network operators continues. **T&MW**

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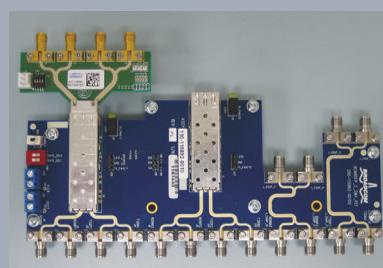
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## Calibrate before testing

Module and host compliance test boards provide your test equipment with access to SFP+ modules and hosts where you can inject signals and make measurements. Because of the high data rates, signals will lose integrity as they travel along the board's copper traces. Thus, you need to account for amplitude losses and increased jitter when characterizing a transmission channel, host board, or module.

Calibration lets you measure the amount of amplitude loss and jitter added from a compliance test board. SFF-8431 section D.11.4 provides a calibration procedure and a test-setup diagram.

"To calibrate a host compliance board, you need to insert it into a module compliance test board," said Lindsay. "That provides access to pattern generators, filters, and jitter sources on one side and oscilloscopes on the other side through SMA connectors." Using the SFF-8431 procedure, you'll be able to calibrate your test signals for amplitude, jitter, and noise.—Martin Rowe



Inserting a host compliance board (green board) into a module compliance board (blue board) provides SMA connectors for signal sources and measurement equipment for calibration.

Courtesy of ClariPhy Communications.

tions and information exchange between systems—Local and metropolitan area networks—Specific requirements Part 3: Carrier Sense Multiple Access with Collision Detection (CSMA/CD) Access Method and Physical Layer Specifications, Amendment 2: Physical Layer and Management Parameters for 10 Gb/s Operation, Type 10GBASE-LRM, IEEE. standards.ieee.org/getieee802.

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## Agilent enhances WiMAX drive test

Agilent Technologies has announced a new software option—labeled E6474-655—for its E6474A network optimization platform that turns a standard WiMAX PC card or other commercial WiMAX CPE (customer premises equipment) into a handheld WiMAX scanning tool for drive test. The software gives network equipment manufacturers and wireless operators' RF engineering teams a cost-effective way to confirm WiMAX coverage and perform basic troubleshooting tasks to assess signal quality.

With the software, a single WiMAX CPE can be used either in "phone" mode or in "scanning mode," providing dedicated RF measurements on up to 10 channels. Phone mode can be used to validate WiMAX service performance; scanning mode assesses WiMAX coverage and signal quality. The same software license used for the WiMAX scanning mode also enables WiMAX measurements using an Agilent W1314A receiver (shown at left in the photo).

Base price: \$15,600. Agilent Technologies, [www.agilent.com](http://www.agilent.com).

## Measure current in the calibration lab

Fluke's A40B precision current shunts let metrology and calibration labs produce current measurements from 1 mA to 100 A, producing 0.8 V at rated current. Comprising 14 shunts with cables and connectors, the A40B series can be used to measure AC or DC current with a precision voltmeter, AC measurement standard, AC/DC transfer standard, or thermal voltage converter.

The A40B set consists of four enclosed shunts (1 mA to 50 mA) and 10 radial shunts in three sizes: small (100 mA to 2 A), medium (5 A to 20 A), and large



(50 A to 100 A). The shunts use a fin design to minimize thermal drift and interference from external magnetic fields. Their low inductance lets the shunts operate from DC to 100 kHz with minimal phase distortion.

Prices: individual shunts—\$1850 to \$9995; set of 14 shunts with cables, adapters, and a transit case—\$47,495. [Fluke](http://www.fluke.com), [www.fluke.com](http://www.fluke.com).

## Instrument senses temperature and humidity

Omega's ETF012 electronic hygrotherm senses the ambient temperature and relative humidity when mounted in an enclosure containing electrical or electronic components. It can turn on a fan or heater at high- or low-temperature set points, helping prevent the formation of condensation in the enclosure. LEDs integrated in the adjustment knobs indicate device operation. The 77x60x43-mm product weighs approximately 0.20 kg (7.1 oz) and is equipped for 35-mm DIN rail mounting. The ETF012 series is CE compliant. Operating temperature range is 0 to 60°C.

Base price: \$90. [Omega Engineering](http://www.omega.com), [www.omega.com](http://www.omega.com).



## Keithley debuts 8x8 MIMO test system

Keithley Instruments has introduced an 8x8 MIMO system that targets primary research of next-generation RF MIMO devices and technologies such as 4G LTE (long term evolution) and UMB (Ultra Mobile Broadband). The new system builds upon 4x4 MIMO test equipment that the company introduced in late 2007.

Keithley MIMO RF test systems are built on the company's RF signal-generator and -analyzer platforms that include Model 2820 RF VSAs (vector signal analyzers), which have a frequency range of 400 MHz to 6 GHz; Model 2920 RF VSGs (vector signal generators), which can generate frequencies from 10 MHz to 6 GHz; Model 280111 WLAN 802.11n signal-analysis software, which provides a measurement suite for analyzing single- or multiple-channel RF devices with up to 4x4 MIMO configurations; and Model 2895 MIMO synchronization units, which provide precise and stable sig-



> > > > > >

nal alignment. The new 8x8 system holds signal sampler synchronization to within  $\pm 1$  ns; sample jitter is less than 1 ns peak-to-peak, and RF-carrier phase jitter is less than 1° peak-to-peak.

Base prices: Model 2820—\$25,000; Model 2920—\$23,000; Model 2895 synchronization unit—

\$9900. Keithley Instruments, [www.Keithley.com](http://www.Keithley.com).

## IR thermometer uses visible light camera

The Extech/FLIR i40, i50, and i60 infrared thermometers feature a visible-light camera that lets you see

the target and point the instrument. The i40 has a 0.6-Mpixel camera, while the i50 and i60 have 2.3-Mpixel cameras. All models feature a picture-in-picture display with fixed (i40), three-step (i50), or scalable (i60) images on a 3.5-in. LCD. With the i40, you can view the target image; the i50 and i60 include a semiconductor laser target, and the i60 is able to display the laser on the screen. The instruments can also find the hottest or coldest spot within a designated area and mark that area.



Temperature range on all three models is  $-20^{\circ}\text{C}$  to  $350^{\circ}\text{C}$  ( $-4^{\circ}\text{F}$  to  $662^{\circ}\text{F}$ ) with  $\pm 2\%$  accuracy and 0.1°C thermal resolution. All models include a 1-Gbyte SD storage card that can store up to 1000 jpg images. The thermometers can run up to 5 hr on a rechargeable lithium-ion battery. Extech Instruments, [www.Extech.com/iseries](http://www.Extech.com/iseries).

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## DTVinteractive unveils ATSC-M/H signal generator

To support the ATSC-M/H (Advanced Television Systems Committee Mobile and Handheld) standard, DTVinteractive offers the ATX2000 signal generator, which integrates a real-time software multiplexer capable of handling mainstream, mobile audio/video, data, and ESG (Electronic Service Guide) packets. The ATX2000 can be used for ATSC-M/H chipset hardware and software development, broadcast engineering simulation, middleware development, receiver R&D, and product manufacturing.

The instrument provides high-quality RF performance, an embedded operating system, an 8.4-in. TFT color LCD touch screen, a USB port, and an RS-232 interface, as well as optional analog I/O output, AWGN (additive white Gaussian noise), and fading modules. RF specifications include an adjustable

output frequency of 50 MHz to 870 MHz with a resolution of 1 Hz. Power consumption is less than 300 W from a 100-VAC to 250-VAC supply (50/60-Hz).

DTVinteractive, [www.dtvinteractive.com](http://www.dtvinteractive.com).

### **PXI embedded controller increases speed to 2.53 GHz**

National Instruments reports that its PXI-8108 embedded controller for PXI and CompactPCI systems offers a 25% performance improvement over the dual-core PXI-8106, and a 2X performance improvement over the single-core PXI-8196. The new controller features a 2.53-GHz Intel Core 2 Duo T9400 dual-core processor and 800-MHz DDR2 memory.

The PXI-8108 works with LabView 8.6 software as well as with LabView Real-Time and LabWindows/CVI Real-Time modules. It can be upgraded to include a 32-Gbyte PXI solid-state hard drive in place of the standard rotating magnetic disk drive. When paired with the solid-state drive, the PXI-8108 offers an extended operating temperature range of 0 to 55°C.

Base prices: PXI-8108—\$4999; solid-state hard drive—\$449.

National Instruments, [www.ni.com](http://www.ni.com).

### **Measurement Computing releases PCIe DIO boards**

Measurement Computing recently released PCI Express versions of two of its PCI digital I/O boards. The PCIe-DIO24 provides 24 channels of digital I/O with selectable 3.3-V and 5-V logic levels. The PCIe-DIO96H, a 5-V-compatible digital I/O board, furnishes 96 bidirectional I/O channels in four independent port groups. Each group is divided into two 8-bit ports and two 4-bit ports. Outputs of the PCIe-DIO96H are high-drive TTL that can source 15 mA and sink 64 mA.

Both of the RoHS-compliant I/O boards offer software-selectable pull-up and pull-down resistor configurations and 82C55 mode zero emulation. Digital I/O lines are accessed through a 37-pin D-type connector on the PCIe-DIO24 and through a 100-pin connector on the PCIe-DIO96H.

The PCIe-DIO24 is connector- and software-compatible with the company's PCI-based PCI-DIO24 and ISA-based CIO-DIO24 boards, for seamless migration of existing applications. Similarly, the PCIe-DIO96H is connector- and software-compatible with the company's PCI-based PCI-DIO96H board. Since the boards are com-

pletely plug-and-play, there are no switches or jumpers. In addition, they are supported by the same external relay and solid-state I/O module racks as their predecessors.

Prices: PCIe-DIO24—\$199; PCIe-DIO96H—\$349. Measurement Computing, [www.measurement-computing.com](http://www.measurement-computing.com).

(continued)

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## EXFO software examines 40G network operation

A new software release for analyzer modules in EXFO's Transport Blazer and Power Blazer product lines gives insight into 40G network equipment behavior, network service operations, and network management system configuration. The software enables the analyzers to perform a host of new tests (including automatic protection switching and service disruption time tests) to ensure compliance with Telcordia GR-253 and ITU-T G.841 specifications.

The software update provides 40G round-trip delay analysis to measure network latency—an important parameter for delay-sensitive traffic such as video. It also provides error/alarm injection for evaluating the behavior of 40G network equipment and carrier NMS (network management software) configurations. This feature sends periodic bursts of errors and alarms to vali-

date that 40G network equipment properly reports recurring network issues and that the NMS is properly configured to handle these issues.

*EXFO Electro-Optical Engineering, [www.exfo.com](http://www.exfo.com).*

## BNC digital delay generator furnishes eight timing channels

The Model 725 digital delay generator from Berkeley Nucleonics synchronizes complicated test setups, providing eight timing channels with programmable logic, unique timing modes, and 10-ns resolution. You can use the Model 725 to synchronize cameras, lasers, shutters, choppers, solenoids, or igniters.

The generator accepts a variety of inputs, including logic signals, switches, transducers, interlocks, computer commands, and gauges. In addition to eight inputs, the Model 725 has eight outputs and eight separate timers. Each of the eight logic

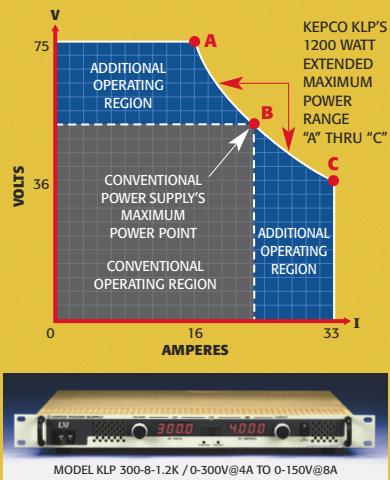
channels can operate independently, functioning as a clock, delayed trigger, or counter. You can use the generator's internal clock or an external clock, as well as select the time base that each channel uses.

The Model 725 hardware controller operates in stand-alone mode or via computer control. You can use the embedded, compiled software, called timerPRO, or LabView to create control schemes. A Windows-based interface lets you program each experiment, channel by channel. In stand-alone mode, the Model 725 can store and recall up to 64 complete settings, with triggering and monitoring done from the unit's front panel. You can design experiments offline and then embed the controller in your test environment for automated operation. Firmware is field-upgradeable, allowing access to new timing modes and capabilities as they become available.

*Berkeley Nucleonics, [www.berkenucleonics.com](http://www.berkenucleonics.com).*

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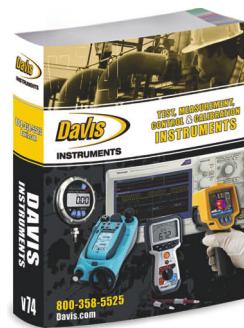
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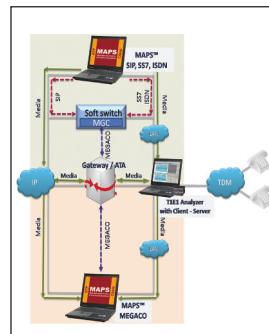
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# MACHINE-VISION & INSPECTION

## TEST REPORT

# CMOS cameras rival their CCD cousins

By Ann R. Thryft, Contributing Technical Editor

**T**he resolution of cameras based on cost-effective CMOS image sensors has continued to improve. Newer sensor technology has led to better light-sensitivity levels and has helped reduce noise levels in the CMOS-based cameras that are penetrating high-speed machine-vision applications. Al Sabeh, VP of sales and applications for Toshiba Teli, explained some of the improvements in CMOS cameras and the sensors on which they are based.

**Q: Where are CCD cameras still used in machine vision?**

**A:** Today, the major difference in usage between CMOS and CCD cameras for machine vision occurs in situations where light levels are very low. In those cases, you still need CCD sensor technology because it is more sensitive to light: The minimum sensitivity for CCD cameras is 1 lux, but for CMOS it's 5 to 10 lux.

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But if there's sufficient illumination during inspection, CMOS camera performance is excellent. And that's the case with the majority of machine-vision applications, since they are usually well lighted. Also, some applications that need a higher near-infrared response, like about 900 to 1000 nm, will require CCD cameras, because those cameras are more sensitive at a higher spectrum.

Traditionally, CCD technology has also delivered lower noise levels, or a higher SNR (signal-to-noise ratio).

**Q: What are the benefits of CMOS cameras?**

**A:** For one thing, CMOS sensors are less expensive than their CCD counterparts. So, for some customers, if CMOS technology meets their sensitivity needs, that's what they will use.

But at least as important is the ability of CMOS cameras to increase frame rates by letting users choose a smaller, lower-resolution area within the image—a window of interest—and sending out only those pixel addresses. Let's say you have a 1020x768-Mpixel camera, but you're interested in an area that's 700x500 Mpixels. On a PC, you can set the camera to that resolution and select the rectangle anywhere on the monitor. So, you can view that area of interest while also increasing camera speed.

For example, our 12-Mpixel CleverDragon camera's window-of-interest feature can be programmed to display a maximum of 28 square



**Al Sabeh**  
VP of sales and applications  
Toshiba Teli

windows within a single image. The camera can perform at 4096x3072-pixel resolution, at 25-fps full-frame speed, with an SNR greater than 54 db. No 12-Mpixel CCD camera will do that. They can only give you 5 fps at that resolution.

**Q: Why did Toshiba Teli design its own proprietary image sensor instead of using a commercially available chip?**

**A:** A CMOS image sensor lets you set the camera to any resolution you want, including lowering the resolution to increase speed. We designed our 12-Mpixel, 1.9-in., CMOS monochrome progressive-scan sensor to be extremely flexible. For instance, you could set our 12-Mpixel camera to 2000x2000 pixels and get 30 fps.

We also designed it for higher performance because there are emerging applications in machine vision and inspection that will demand that performance. A major example is the industry move from 6-in. to 12-in. wafers. Now those bigger wafers can be inspected at much faster speeds. □

## EDITOR'S NOTE

## Machine vision's changing times

By Ann R. Thryft  
Contributing Technical Editor

As I've talked with vendors, analysts, and industry observers to learn more about the state of the machine-vision industry, what has struck me is how energetic and forward-looking everyone is.



This industry is experiencing major changes, including maturing markets, price erosion, and simultaneous demands for higher resolution and bandwidth while process technologies shrink and new materials come into play. But there's also a huge amount of creativity being aimed at these challenges, and much of it was on display at Semicon West (see facing page).

Nearly every corner of the industry is harnessing new technologies, or new uses of existing technology. These include the increasing use of 3-D paste inspection for high-reliability and complex parts, the growing role of software, and new high-resolution capabilities of scanning electron microscopes that put these systems into another class altogether (see p. 66).

The digitization trend, such as in camera sensors, and open industry standards bring more flexible and scalable systems, improved interoperability, and ultimately lower costs. They also bring open platforms. And with digitization, open platforms, and standardization comes greater connectivity, such as the GigE Vision interface (see p. 64).

It's an exciting time to be in machine vision and inspection. □

Contact Ann Thryft at [ann@tmworld.com](mailto:ann@tmworld.com).

## HIGHLIGHTS

## Microscan acquires Siemens' M-V business

In September, Microscan announced plans to acquire the Siemens Machine Vision business, which was originally Acuity CiMatrix, the company that developed the 2-D Data Matrix code. Microscan, a manufacturer of precision data-acquisition and control products used in the electronics, life sciences, and automotive industries, plans to keep the division's headquarters in Nashua, NH, open and to retain the majority of the workforce.

"Vision products for identification and inspection are a growing aspect of the precision data-acquisition and control market," said Jeff Timms, president of Microscan. "The acquisition of the Siemens Machine Vision business brings with it a depth of expertise in Data Matrix and vision product design that is second to none. Combined with Microscan's deep experience in data-acquisition solutions, the purchase of this business tremendously augments our product portfolio and brings with it a

unique and complementary offering to our customers."

According to Dennis Sadlowski, president and CEO of Siemens Energy & Automation, Siemens will continue to produce industrial identification (Auto ID) and RFID code-reading systems. [www.microscan.com](http://www.microscan.com).

## Stemmer announces CVB version 10

Stemmer Imaging has introduced version 10 of its Common Vision Blox (CVB) programming library. In addition to CVB's hardware independence and connection flexibility, Version 10 includes a new installation routine and support for the 32-bit version of Microsoft Windows Vista.

The Version 10 installation procedure makes system restarts unnecessary, even after the installation of the hardware drivers. Once the software is installed, all system settings can be accessed via a central management console.

The update is free for registered users of Common Vision Blox, and a free 14-day full version is also available for evaluation. [www.commonvisionblox.com](http://www.commonvisionblox.com).

## Zeiss rolls out electron microscopes

Carl Zeiss SMT has launched a new SEM (scanning electron microscope) as well as an argon ion beam column for its NVision 40 CrossBeam nanoscale workstation. Based on the company's Gemini field-emission technology, the new Sigma SEM accommodates specimens up to 250 mm in diameter and 145 mm tall and performs material analysis at high resolution using both energy-dispersive and wavelength-dispersive x-ray spectroscopy techniques. In addition, its coplanar chamber design allows simultaneous energy dispersive x-ray spectroscopy and electron backscattered diffraction.

To enable the production of highly polished TEM (transmission electron microscope) lamellas, Zeiss offers an argon ion beam column that can be retrofitted to the NVision 40 CrossBeam workstation. This third column enhances sample quality by almost completely removing surface damage that typically occurs during the initial FIB (focused ion beam) milling steps. The NVision 40 Argon is available in two models: a process-oriented, high-throughput version for preparing routine TEM samples for semiconductor customers and a multipurpose model for processing and analytic applications in materials science and in the semiconductor lab. [www.smt.zeiss.com](http://www.smt.zeiss.com).

# Cameras, Frame Grabbers, & Software

## Vision and inspection products focus on higher resolution, faster processing

Semicon West, San Francisco, CA, July 15–17, SEMI. [www.semiconwest.org](http://www.semiconwest.org).

**Qioptic Imaging Solutions** showed the compact A-Zoom Micro probing microscope, which streamlines PCB (printed-circuit board), semiconductor, and flat-panel display probing. The company also showed its programmable Fetura advanced-zoom imaging lens that provides zoom magnifications of 0.52X to 6.5X, covers a 12.5:1 zoom range in 500 ms, and includes multiple interfaces for OEM integration.

Aiming at applications that need a portable microscope system, **Hirox USA** introduced its KH-7700 system that integrates a digital camera, a light source, a computer, an LCD monitor, and software. The system blends information from multiple exposures to produce a wider dynamic range than can be accomplished with other digital imaging techniques.

Targeting optical inspection and quality control, **Leica Microsystems** showed several microscopes and macrosopes. The company's Z16 macrosopes have a 16:1 zoom range and provide zoom magnifications of 0.57X to 9.2X. Leica's DM6000 automated digital microscope systems can be used with all incident light methods and are designed for use in R&D labs.

**FEI** debuted the XHR SEMs (extreme high-resolution scanning electron microscopes), which provide subnanometer resolutions and use very low beam energies to avoid distortions caused when the beam penetrates the material underneath the sample (see p. 66). The Magellan 400L model, optimized for semiconductor labs, can view critical details with clarity and contrast on complex 3-D structures in 32-nm nodes and below.

**Surface Imaging Systems** introduced its NanoStation 300. The system augments atomic force microscopy (AFM) with optical inspection capability to rapidly identify regions of interest. **Viscom** exhibited its MX100IR desktop system, which uses transmitted and reflected infrared to inspect wafers. **Nikon Instruments** introduced two new systems. The WES-3000 inspection tool makes it easier to inspect wafer edges, where defects have proliferated and become more complex along with the increased use of immersion lithography. The APM-3000 series leverages a form of birefringence in a Fourier space to detect critical dimension and pattern edge roughness variations in wafers.

**Machine Vision Products** exhibited its Ultra 850G modular AOI (automated optical inspection) system for packaging and semiconductor inspection, used primarily in flux paste, die placement, component, and underfill processes. **Matrox** demonstrated the Matrox Imaging Library 9.0, which is tailored for high-throughput, processing-intensive applications such as wafer and mask inspection, and is designed to take advantage of high-performance computing clusters based on graphics processor units.

The new surface-mount device and chip-on-board versions of the high-brightness LED light-line products from **Schott Fiber Optics** offer high luminosity beams for better contrast in applications such as surface inspection. Schott also showed its new LLS LED light source for machine-vision devices, which runs on less than 15 W and has a 50,000-hr lifetime.

At the InterSolar North America show co-located with Semicon West, **KLA-Tencor** exhibited its new P-6 surface-profiler system, a bench surface-metrology system for samples up to 150 mm. It applies semiconductor profiler system technology to scientific research and production environments, such as photovoltaic solar cell manufacturing.—*Ann R. Thryft*



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# GigE Vision expands in machine vision

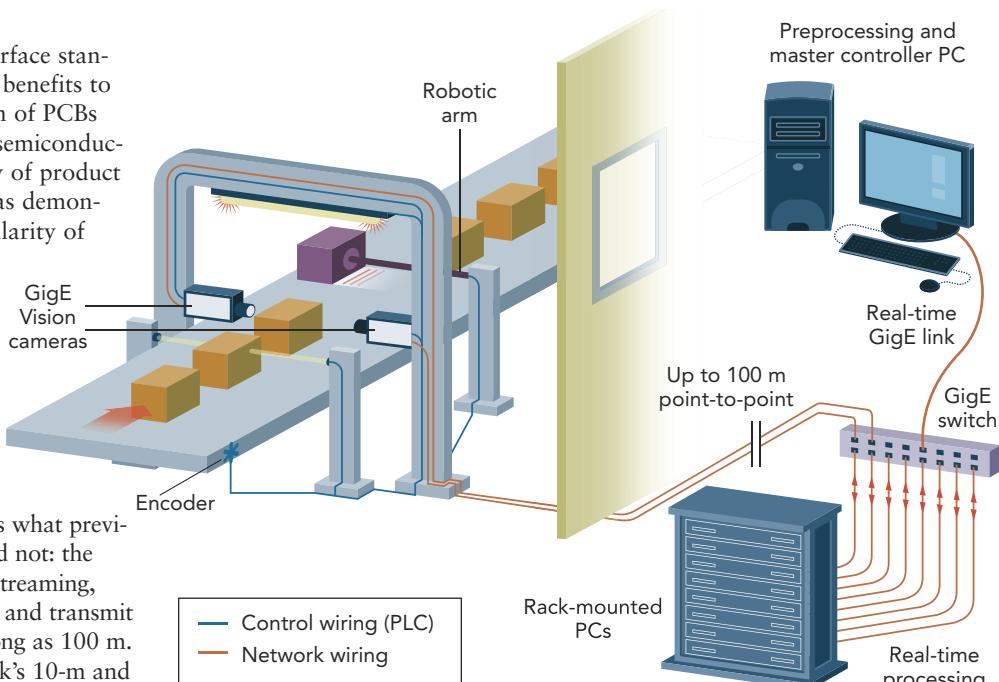
By Ann R. Thryft, Contributing Technical Editor

The GigE Vision interface standard brings several benefits to machine-vision inspection of PCBs (printed-circuit boards), semiconductors, and wafers. A flurry of product introductions this year has demonstrated the growing popularity of the interface in machine-vision cameras, from small embedded boards to two-box, 12-Mpixel cameras (see "Machine-vision cameras get GigE," p. 65).

Perhaps GigE Vision's main benefit is its 125-Mbps speed, which allows what previous Ethernet standards did not: the ability to reliably handle streaming, uncompressed image data and transmit that data over cables as long as 100 m. Compared to Camera Link's 10-m and FireWire's 5-m cable lengths, GigE's longer reach opens up new configuration possibilities for keeping PCs and related image-processing hardware far away from the harsh production line environment. GigE's 100-m cable length—and the ubiquity and low cost of standard Ethernet hardware, cables, and connectors—makes that possible without repeaters or extenders.

These aspects of GigE also make it possible for manufacturers to set up control centers where images are processed in multiple, clustered PCs, said Eric Carey, R&D director for Dalsa Montreal. "Some of our customers are considering using a GigE Vision link to transfer images to a control center for processing," he said.

But when you send GigE camera data to an Ethernet switch and then to the PC, bandwidth can't be guaranteed and packet loss is likely. "With higher-bandwidth cameras, you need to be careful about aggregating camera bandwidth so you don't overload the link," Carey said. "So, most customers are presently implementing a point-to-point connection."



**In this example of a manufacturing line, images are sent over an IP network using standard Category 5 or 6 Ethernet cables to a control room where rack-mounted servers process them in real time.** Courtesy of Pleora Technologies.

Ethernet's multicast capability is what makes it possible to decouple image acquisition at the camera from image processing at the PC, said George Chamberlain, president of Pleora, a co-founder of the GigE Vision standard. "In a LAN, multicast capability lets you send video data simultaneously from one source to multiple locations," he said. "Processing, archiving, monitoring, or even additional processing, perhaps using multiple PCs, can be done at multiple locations." He added that using FPGAs (field-programmable gate arrays) instead of DSPs (digital signal processors) to perform image processing can make a multicast solution more scalable, less expensive, and simpler to develop.

GigE Vision is also scalable to accommodate networks operating on the 10 GigE standard, and it eliminates frame grabbers, which can cost as much as \$3000 depending on func-

tionality, said Ravi Guntupalli, business manager for Princeton Instruments' imaging division. He explained that upgrading a network to handle GigE Vision in the first place and coping with the loss of frame grabbers can each pose separate design challenges.

Since frame grabbers traditionally handle image processing, eliminating them increases the load on the host CPU, adds image-processing CPU cycles, and decreases the number of CPU cycles available for object recognition and registration. Guntupalli said that using cameras with built-in image-processing capabilities can help reduce the CPU load considerably. In Princeton's MegaPlus line, for example, those capabilities include RGB color interpolation, flat-field formalization, and defect correction. Implementing them with FPGAs instead of DSPs, as Princeton has, can reduce time, cost, and programming effort, he said.

# IMAGING solutions.



Alternatively, the task of converting GigE Vision packets into usable images can be offloaded from the host CPU by using a general-purpose co-processing board and a NIC (network interface card) on the PC's PCI Express bus, said Carey. "Many of our customers are still using typical analog cameras with a frame grabber and a dedicated link, so aggregating is a new concept," he said. "It becomes easy to scale a system and easy to try to do too much, so you need to be aware of the average bandwidth that can be sustained on the link." In many inspection systems, this bandwidth is still only about 10 to 15 Mbps, so multiple cameras can be handled with a NIC.

Of course, modifying an existing network to take advantage of the GigE Vision standard can be an issue with cameras, because sensors are more expensive components than interface electronics, yet they don't need to be swapped out nearly as often, said Guntupalli. One way to address this problem is to place the bus-interface electronics in one box and the more-expensive image sensor electronics in another. You can swap out the inter-

face and use the camera head with whatever interface you choose. "At resolutions of around 11 or 16 Mpixels, sensor prices will not be coming down that much because volumes are lower, and because the amount of silicon used is a lot more," Guntupalli said.

Princeton is one vendor that has taken this approach in its MegaPlus line.

Although many manufacturers have accepted the GigE Vision standard and are encouraging widespread adoption, adoption rates have been slow to match initial expectations—as is often the case with new standards. Princeton, for example, expects customers who have complex inspection setups on their PCB production lines to stay with Camera Link because of its high data throughput, said Guntupalli. "But in offline semiconductor wafer inspection, customers have more incentive to use GigE, since their throughput needs are lower and they can benefit from its reduced cost, longer cable length, and ease of use," he said. □

The online version of this article includes a chart comparing the main features of GigE Vision, Camera Link, and FireWire: [www.tmwORLD.com/2008\\_10](http://www.tmwORLD.com/2008_10).

## Machine-vision cameras get GigE

Last spring, Prosilica launched the GB-Series Gigabit Ethernet CCD cameras, which are single-board versions of its GC-Series GigE Vision models. Intended for OEM applications that need machine-vision cameras in a small space, the credit-card-sized GB-Series cameras come in monochrome or color versions and with vertical or inline connection methods. Four models deliver resolutions ranging from VGA to 5 Mpixels and full-resolution frame rates up to 120 fps. Other capabilities include configurable IP addresses and multicasting.

Meanwhile, NET USA introduced the GimaGO family of GigE Vision-enabled, progressive-scan cameras. Offered in 8-bit and 12-bit versions, the cameras are equipped with a variety of CCD image sensors in monochrome and color versions, with resolutions from VGA to UXGA. Also last spring, FLIR Systems debuted the A325 GigE Vision infrared camera, designed for integration into machine-vision systems that require non-contact imaging and temperature measurements.

Other GigE Vision product introductions include Pleora's iPORT NTX-Mini with GigE Vision and Princeton Instruments' existing CCD-based, two-box MegaPlus cameras that are now GigE Vision-enabled. The iPORT NTX-Mini is an embedded, IP in-camera engine, measuring 42x42 mm and dissipating 1.45 W. Ranging from 1.6 to 16 Mpixels, Princeton's MegaPlus cameras feature Camera Link and IEEE 1394a (FireWire) interfaces in addition to GigE Vision.—Ann R. Thryft

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# SEM technology sees below 1 nm

By Ann R. Thryft, Contributing Technical Editor

As semiconductor process geometries shrink to the 32-nm node and below, obtaining clear images and data of critical IC structures is becoming a lot tougher using traditional SEMs (scanning electron microscopes) for surface inspection. Scientists in process-development labs and engineers at logic and memory manufacturers are struggling to quickly see complex 3-D surfaces, as well as materials interfaces and profiles. They also need to see all of this from multiple angles and at resolutions below 1 nm without increasing the electron-beam voltage.

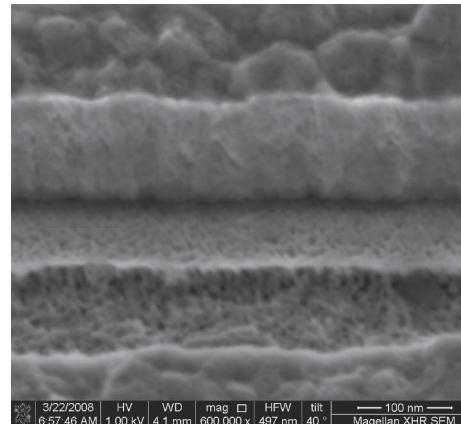
**This XHR SEM image shows a tilted view of a deprocessed logic device sample, imaged at 1-kV beam voltage and 600,000 times magnification.** Courtesy of FEI and STMicroelectronics, Malta/Grenoble.

To address these problems, FEI has begun leveraging techniques and components used in dual-beam systems, which integrate SEM and FIB (focused ion beam) methods. The result is a new class of instruments that the company calls XHR (extreme high-resolution) SEMs. FEI introduced the first such machine, the Magellan XHR SEM, at Semicon West (July 15–17, San Francisco, CA). The new system achieves surface sensitivity and subnanometer resolution at voltage levels from 1 kV to 30 kV.

Traditionally, SEMs have been favored in both semiconductor labs and production facilities for their nanometer-level imaging and ability to handle bulk samples, as well as for their wide imaging range, simple sample-preparation requirements, and analytical capabilities. But just as capturing clear images of smaller features has become more challenging, so has achieving

good contrast on the surfaces of sensitive dielectrics and resists without increasing voltage. Lower voltages are needed to minimize the damage to sample materials. They also avoid the distortions caused when a higher voltage beam passes below the sample's top surface and into the material below, creating artifacts in images.

Solving these challenges with UHR (ultra-high-resolution) SEMs has been difficult, said FEI's Richard Young, technologist for scanning electron mi-

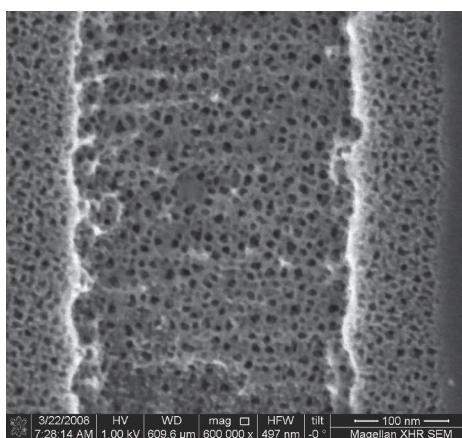


3/22/2008 | HV: 1.00 kV | WD: 4.1 mm | mag: 600,000 x | HFW: 497 nm | tilt: 40° | 100 nm | Magellan XHR SEM

croscope and small dual-beam systems. Some of these machines have stringent sample-preparation requirements.

"Many UHR SEMs are limited to samples less than 10 mm per side and do not allow the rotation and tilt flexibility needed for good examination of edges and interfaces," said Young. "They often require extra preparation steps just to get the sample into the system." Other UHR SEMs use beam voltages of 5 to 10 kV in order to get higher-resolution images.

Due to these constraints, most UHR SEMs are not designed for high sample throughput. Yet, demand for higher throughput is increasing at process-development labs, where scientists work to reduce development time, and at manufacturing support labs, where



3/22/2008 | HV | WD | mag | HFW | tilt | — 100 nm —  
7:28:14 AM | 1.00 kV | 609.6 μm | 600 000 x | 497 nm | -0° | Magellan XHR SEM

**This XHR SEM image shows a top-down optimal working-distance view of a deprocessed logic device sample, imaged at 1-kV beam voltage and 600,000 times magnification.** Courtesy of FEI and STMicroelectronics, Malta/Grenoble.

ages, sample handling constraints, and low throughput. It combines the column, stage, and platform from FEI's dual-beam FIB/SEM products with new technology that permits the system to offer improved low-voltage performance by reducing the electron beam's energy spread. This results in decreased probe size and improved sample contrast, producing rapid surface imaging at tens of images per hour. The machine's 100-mm, high-precision, high-stability, five-axis tilting/rotating stage accommodates large samples or multiple smaller samples,

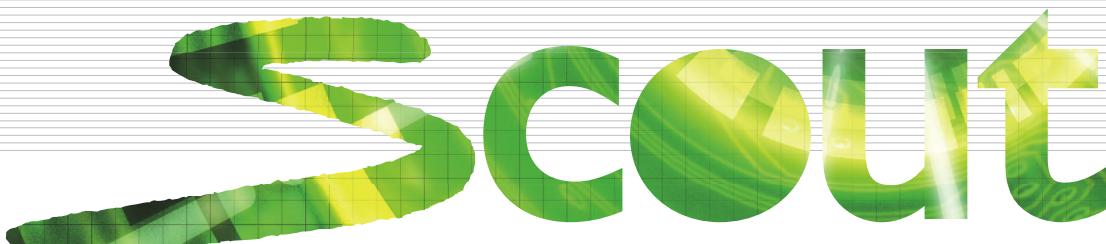
while an optional automated loadlock further improves sample throughput.

Although FEI has pushed its XHR SEM's low-voltage resolution below 1 nm, that doesn't mean that the need for FIBs or TEMs is going away, said Todd Templeton, the company's product marketing manager for scanning electron microscope and small dual-beam systems. FIBs and TEMs may not offer the XHR SEM's combination of features and abilities, but both can reveal defects below the surface in advanced materials and devices. For example, even though TEM samples take longer to prepare and image, TEM systems provide chemical analysis and resolutions as high as 10 times those of the XHR SEM. Both of these capabilities are sometimes needed in process development and failure analysis where engineers need to get more accurate profile and metrology information. □

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### PRODUCTS

#### Point Grey adds USB 2.0 digital cameras

Joining Point Grey Research's line of FireWire digital cameras are models incorporating USB 2.0 interfaces. The new cameras include the Chameleon, which employs a 1.3-Mpixel Sony EXview HAD CCD, and a USB 2.0 version of the Firefly MV. The cameras use an FPGA chip to control exposure, resolution, frame rate, pixel binning, and user memory channels.

*Point Grey Research, [www.ptgrey.com](http://www.ptgrey.com).*

#### SVS-Vistek recorder captures high-speed events

By monitoring high-speed manufacturing lines, the SVMonitor digital image recorder from SVS-Vistek helps engineers analyze and debug the sources of errors in automated processes. The recorder is compatible with cameras incorporating GigE, Camera Link, FireWire, and USB 2.0 interfaces. Both the starting and stopping of a sequence recording can be triggered through a variety of external signals, including those from hardware, software, changes within a picture, or by absolute and relative time.

*SVS-Vistek, [www.svs-vistek.com](http://www.svs-vistek.com).*

#### Basler adds color line-scan cameras

Basler Vision Technologies now offers color versions of its sprint line-scan cameras with resolutions of 2000, 4000, and 8000 pixels. The 2000- and 4000-pixel models have maximum line rates of 70 kHz, while the 8000-pixel camera has a rate of 39 kHz. The cameras are based on a dual-line CMOS sensor that combines the image quality of CCD sensors with the high speed of CMOS. Basler says the sensor has a high quantum efficiency of up to 60%, a fill factor of 100%, and an increased signal-to-noise ratio at low light conditions.

*Basler Vision Technologies, [www.baslerweb.com](http://www.baslerweb.com).*

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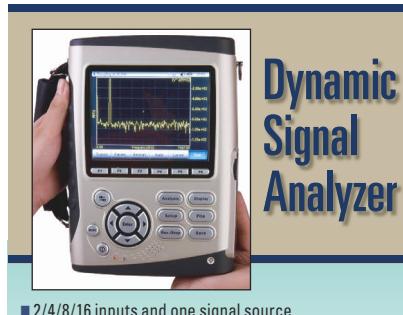
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**JOHN VANNEWKIRK**

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In 2003, John VanNewkirk engineered the acquisition of CheckSum by an investor group, Teton Industries. Earlier, he led a successful turnaround of a steel service center in southern China for Van Shung Chong Holdings (VSC), a public company in Hong Kong. Prior to joining VSC, VanNewkirk served as a management consultant with Bain & Co. in Hong Kong and San Francisco. During his years at Bain, he developed and implemented growth strategies for Fortune 500 companies. VanNewkirk holds a BS degree from Brown University and an MBA from Harvard Business School. Contributing editor Larry Maloney conducted a phone interview with VanNewkirk on new technologies for board test and onboard programming.

## Time to break away from "big iron"?

**Q: How has growing electronics complexity increased the challenges in board test?**

**A:** With surface mount, system-on-chip, and other innovations, density has increased to the point where we often lack sufficient access for test. The result is that in-circuit testers are challenged to provide the 90% coverage we saw years ago. The second issue is the increased use of ISP (in-system programmable) chips, seen in such devices as embedded microcontrollers, flash, and FPGAs (field-programmable gate arrays). Lastly, more manufacturers are building many boards at the same time. Combine these multiboard panels with use of ISP devices and you've got a tremendous manufacturing challenge. It's remarkable that yields in board test have improved substantially over the past decade, despite this complexity.

**Q: What changes do you see in the kinds of defects that crop up?**

**A:** Overall, the number of defects has dropped in half over the last decade, but the make-up of the fault spectrum has changed. Solder-related defects have actually grown significantly over the last 10 years with the predominance of surface-mount and very fine-pitch devices. You also see more mechanical-related defects linked to surface mount. For example, a capacitor might pass an electrical test, yet not be located precisely on the board.

On the other hand, digital device defects, which used to account for up to a third of all defects in the mid-'90s, have declined to almost nothing. In a study of five of its biggest plants, Jabil Circuit found that only one board out of 2200 had a digital device failure.

This data confirms what test engineers already knew when they decided to drop digital vector test. So the question is: How far should manufacturers go in their test investment to catch a defect at ICT (in-circuit test) that occurs so rarely, when the defect will still be caught at functional test?

**Q: In this environment, what is the place of high-end in-circuit testers?**

**A:** The issue I have with these so-called "big-iron" testers has more to do with economics than technology. These testers have been doing a good job for 20 years in catching defects. The problem comes in the pain they cause manufacturers. Fixtures and programming can cost twice as much as they do for lower-cost ICT. You also have issues with maintenance and training, which can be a major problem at plants in developing countries where you often don't have people who have spent months in training courses.

**Q: What keeps manufacturers from opting for lower-cost solutions?**

**A:** There is still a huge group of electronic manufacturers who have an installed base of expensive ICT platforms and are reluctant to try new technologies. They view ICT as a solved problem. Although they may have excess ICT capacity and shrinking profit margins, some of these firms are simply unwilling to change.

**Q: How do you change that mindset?**

**A:** We appeal to the technical needs of engineers and focus on areas that cause pain, such as in-system programming of chips. CheckSum invented the MultiWriter onboard system that can program up to 384 ISP chips at the same time, usually in seconds instead of the minutes required by conventional ICT programmers. For customers that have panels of boards and need high throughput, this is a technique that offers great advantages. MultiWriter has prompted more companies to look at CheckSum, giving us the opportunity to show our other products, such as low-cost ICT platforms. **T&MW**



John VanNewkirk answers more questions dealing with onboard programming and lower-cost ICT systems in the online version of this interview: [www.tmworld.com/2008\\_10](http://www.tmworld.com/2008_10).

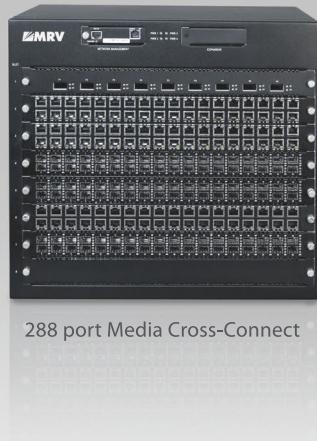
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